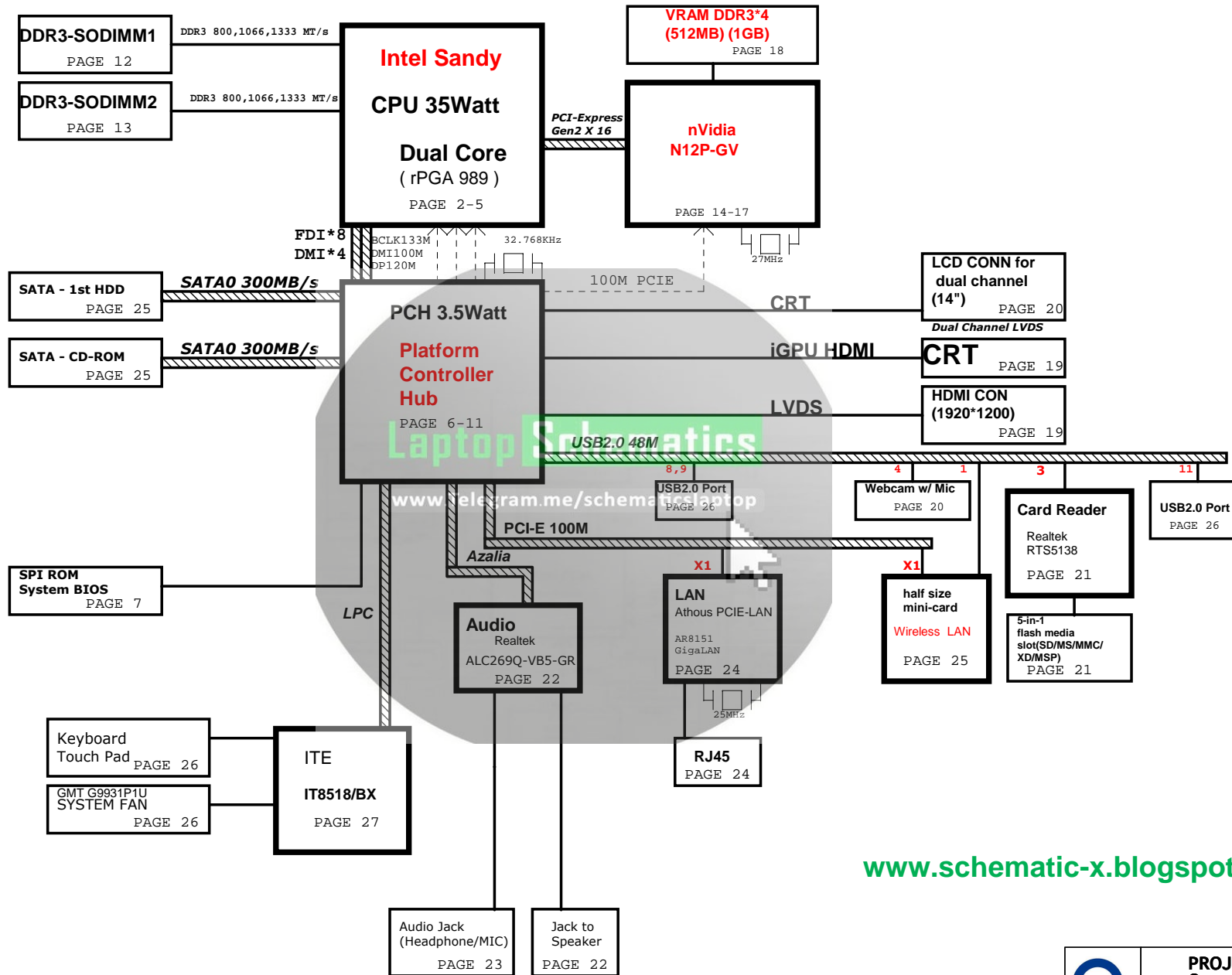


QLC 14" (Huron River) BLOCK DIAGRAM

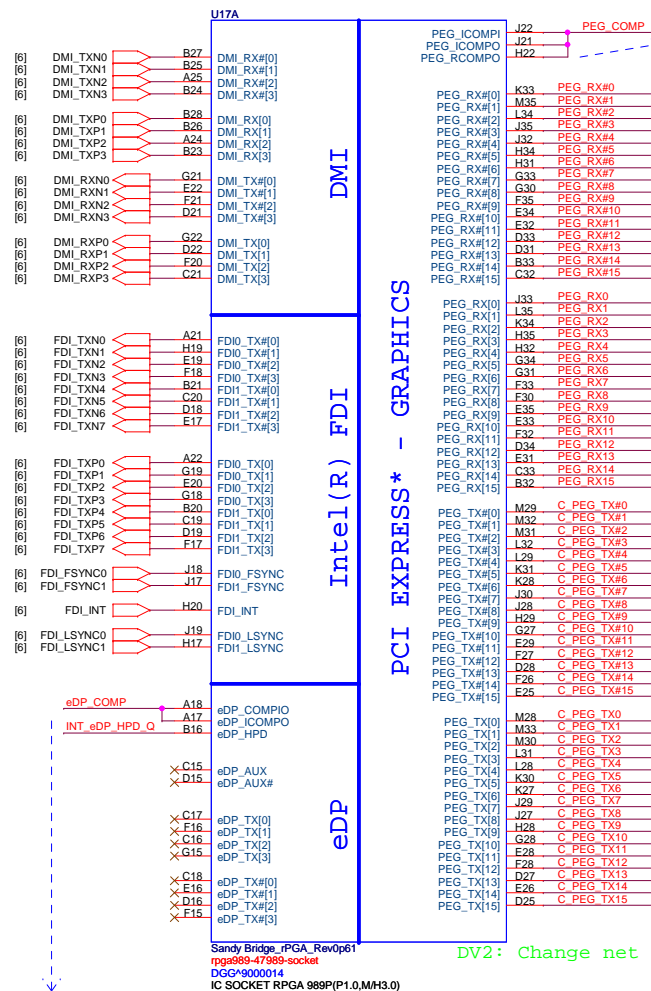
PCB 8L STACK UP

LAYER 1 : TOP
 LAYER 2 : SGND
 LAYER 3 : IN1(High)
 LAYER 4 : IN2(Low)
 LAYER 5 : SVCC
 LAYER 6 : IN3(High)
 LAYER 7 : SGND
 LAYER 8 : BOT



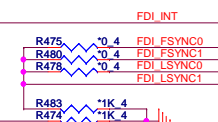
www.schematic-x.blogspot.com

Sandy Bridge Processor (DMI,PEG,FDI)



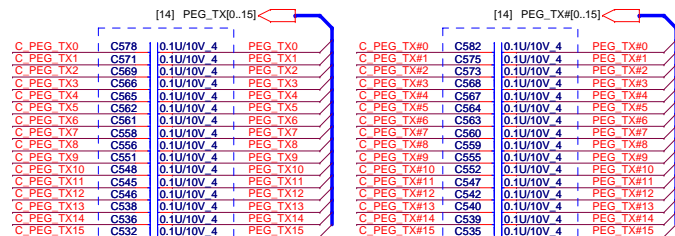
eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

**FDI disable
(DIS only stuff)**



FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

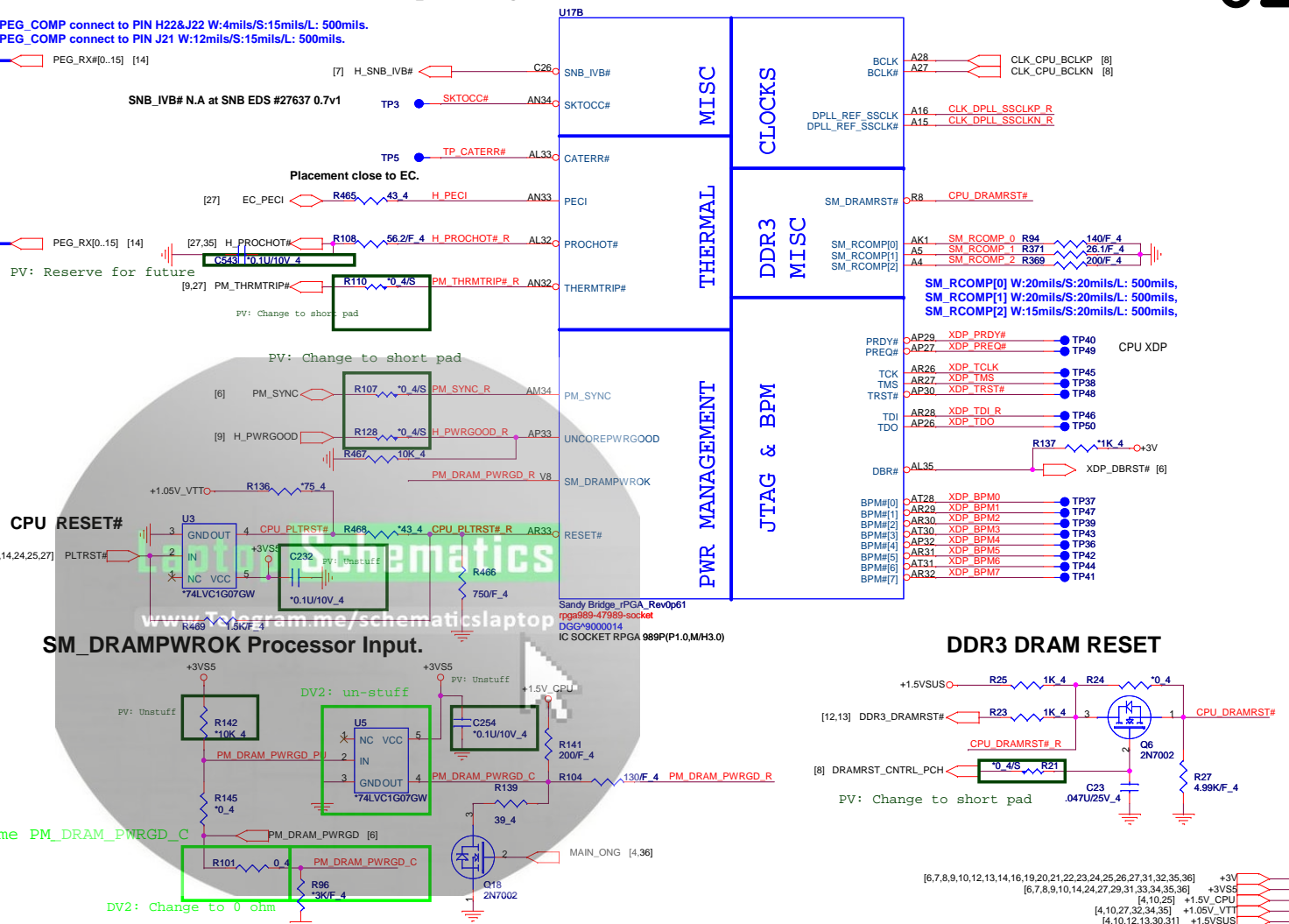
PEG x16 disable (UMA only remove)



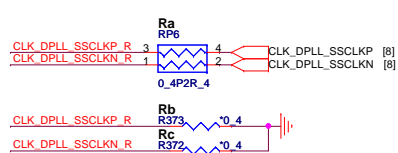
0.22uF AC coupling Caps for PCIE GEN1/2/3

0.22uF AC coupling Caps for PCIE GEN1/2/3

Sandy Bridge Processor (CLK,MISC,JTAG)

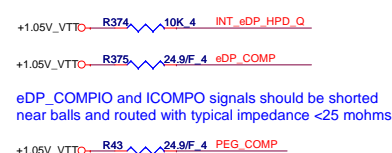


Embedded Display PLL Clock



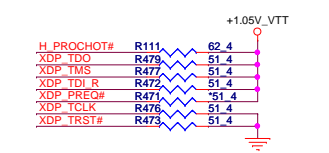
	Ra	Rb	Rc
DIS	NC	Stuff	Stuff
SG/UMA	Stuff	NC	NC

DP & PEG Compensation



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms
PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

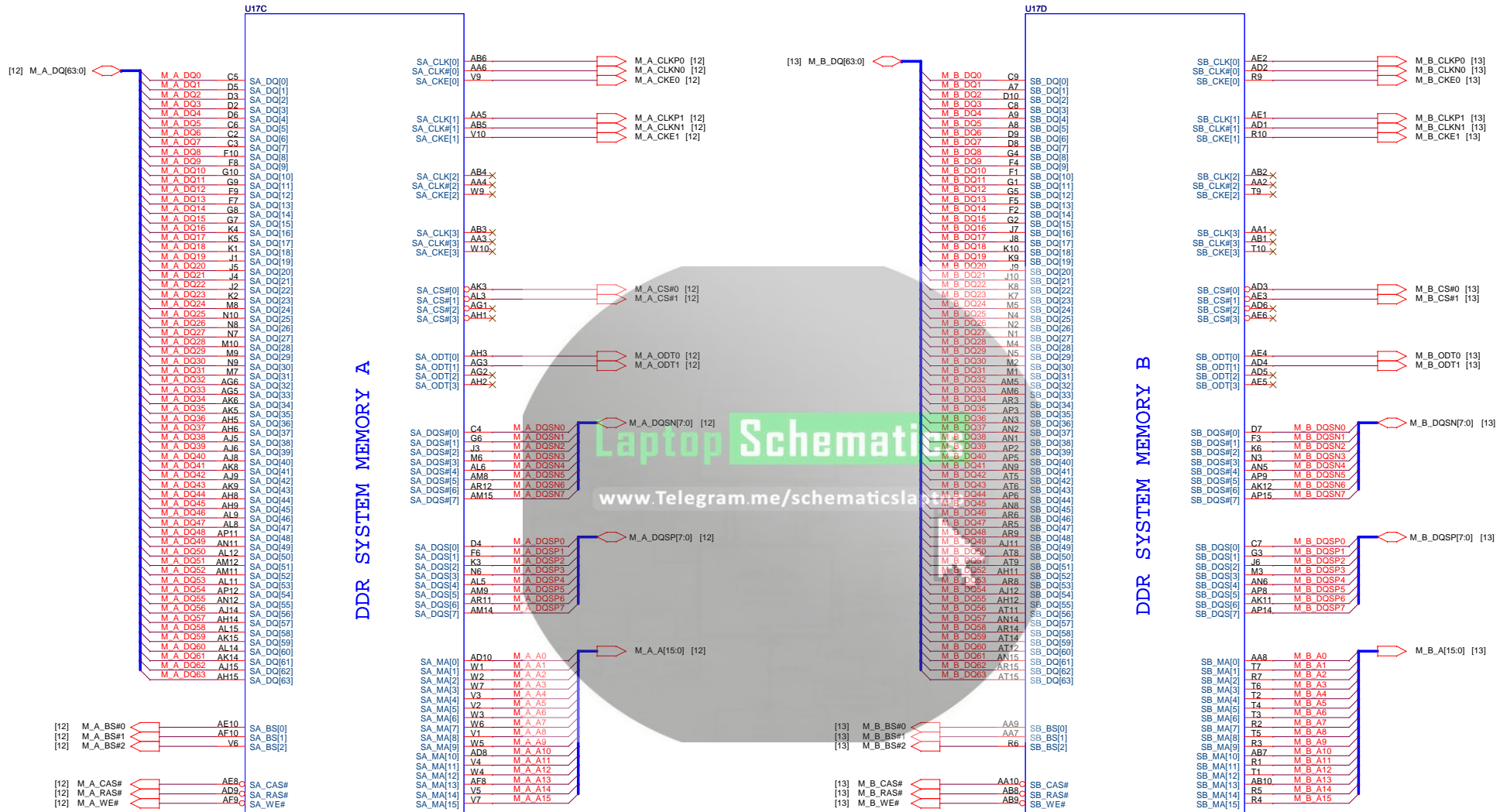
Processor pull-up (CPU)



PROJECT : QLC
Quanta Computer Inc.

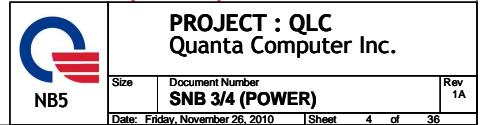
Size	Document Number SNB 1/4 (PCIE&DMI&FDI)	Rev 1A
Date: Friday, November 26, 2010	Sheet	2 of 36

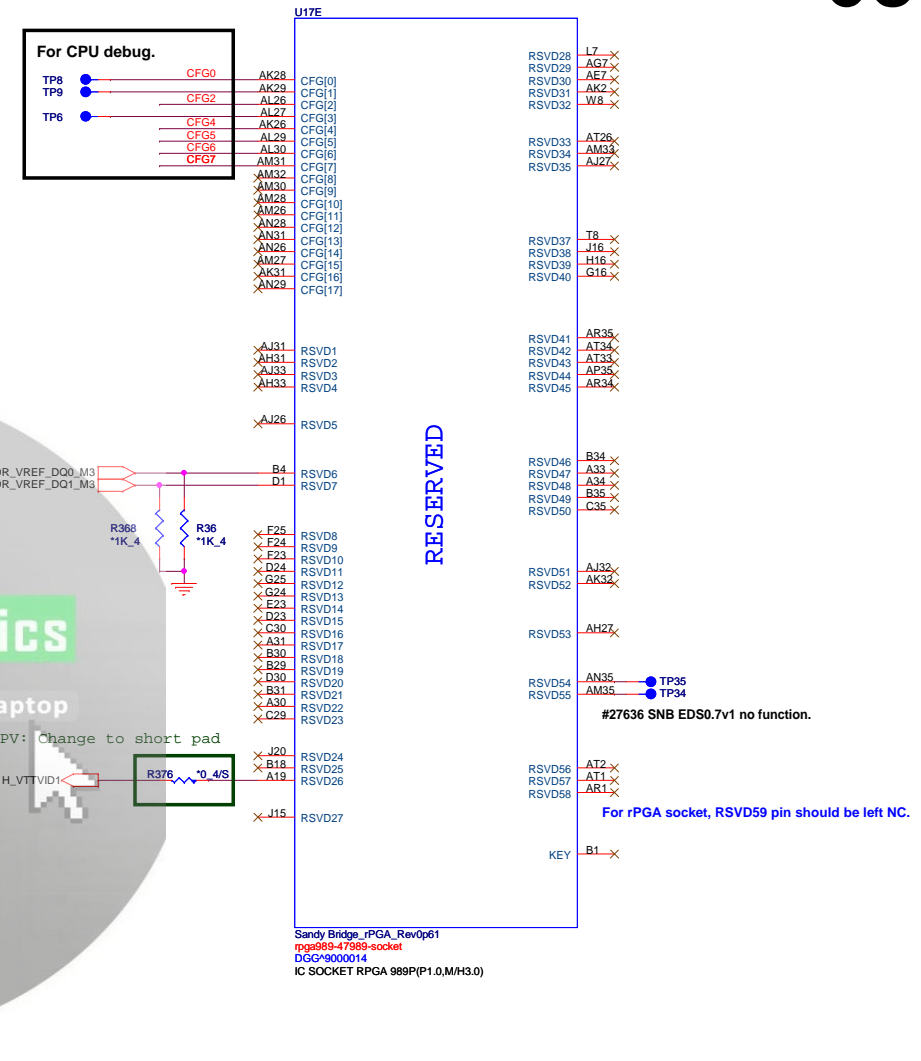
Sandy Bridge Processor (DDR3)




Sandy Bridge_rPGA_Rev0p61
rpg989-47989-socket
DGG-9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

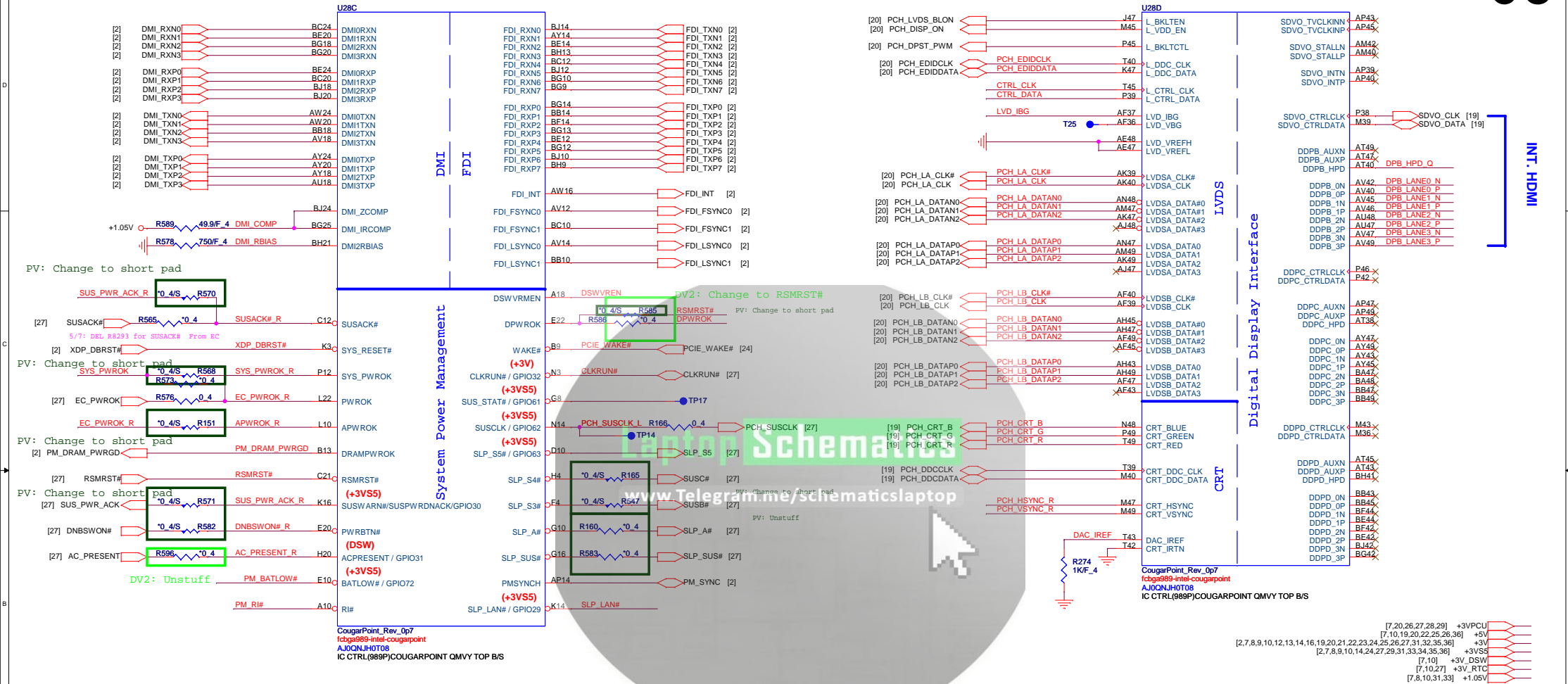
Sandy Bridge_rPGA_Rev0p61
rpg989-47989-socket
DGG-9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)



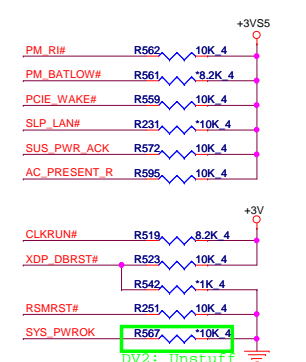


	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

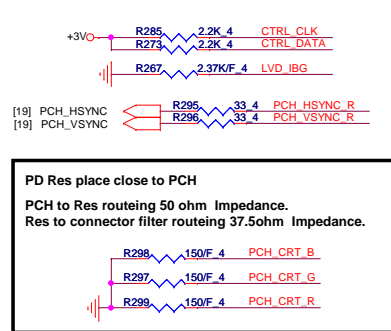
 NB5	PROJECT : QLC Quanta Computer Inc.			
	Size	Document Number		Rev
		SNB 4/4 (GND)		1A
Date	Friday, November 26, 2010	Sheet	5 of 36	



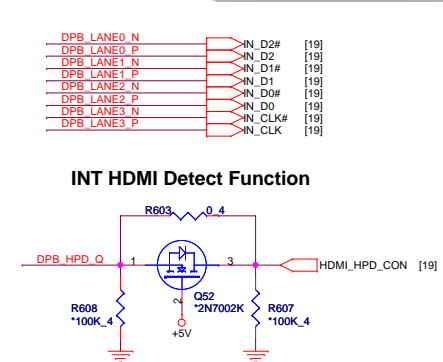
PCH Pull-high/low(CLG)



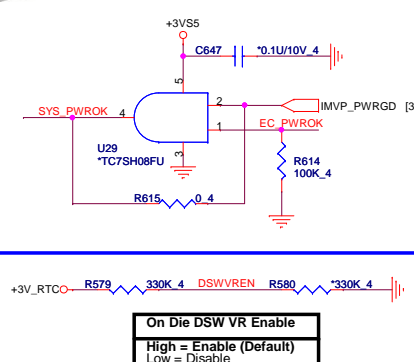
INT LVDS & CRT disable (DIS only remove)



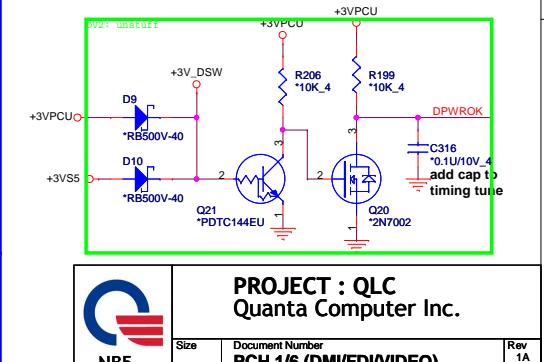
INT HDMI disable (DIS only remove)



System PWR_OK(CLG)

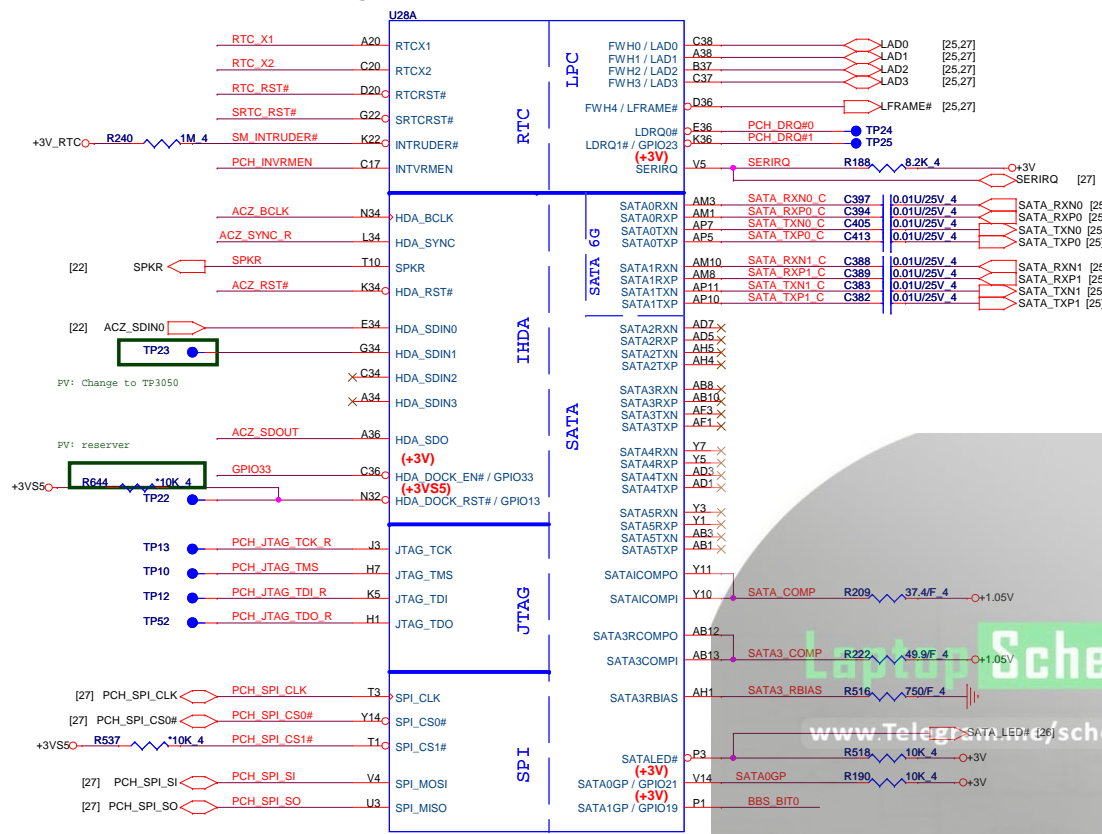


DPWROK FOR DSW

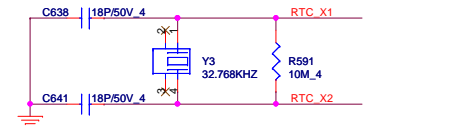


Cougar Point (HDA,JTAG,SATA)

07

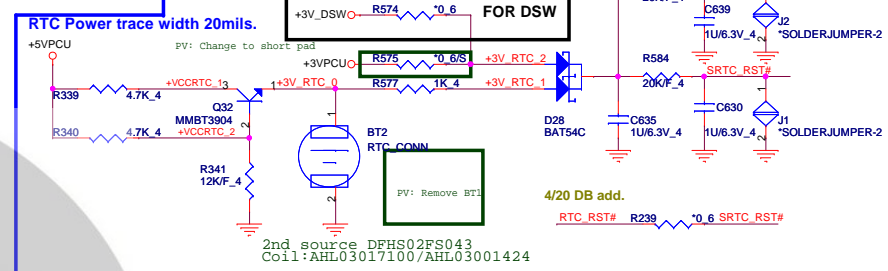


RTC Clock 32.768KHz

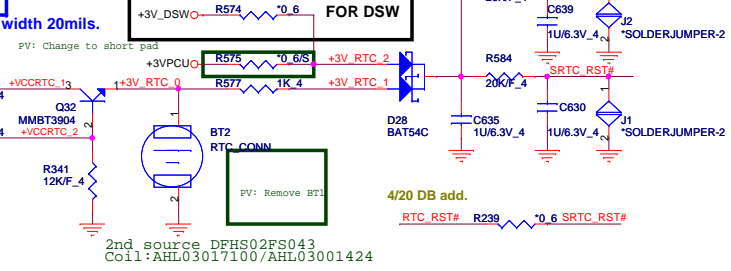


HDD0 (SATA3 6.0Gb/s)

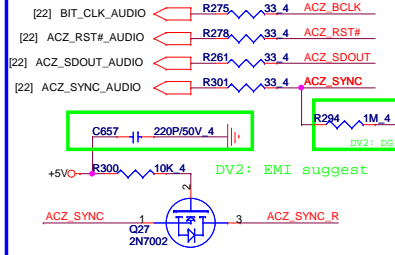
ODD (SATA1 1.5Gb/s)



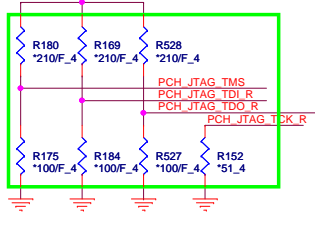
RTC Circuitry(RTC)



HDA Bus(CLG)

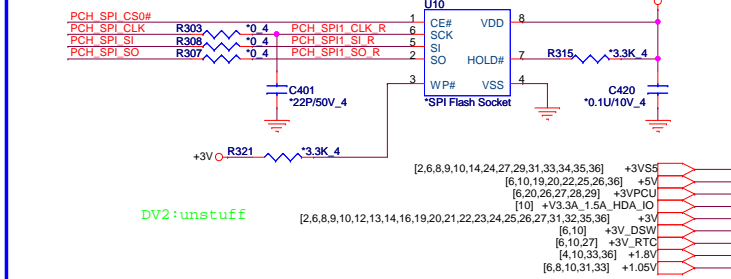


PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)

Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031



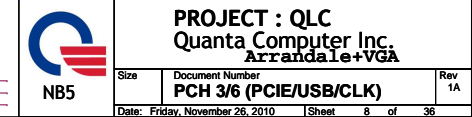
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R185 *1K 4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R292 *1K 4 R290 *10K 4 +3V
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R581 *330K 4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R600 *1K 4 +3V
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	R292 *1K 4 R290 *10K 4 +3V
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	Should not be pull-down (weak pull-up 20K)	R538 *1K 4 R290 *10K 4 +3V
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R212 *1K 4 NV_ALE [8]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm 4/29 modify	+1.8V R548 *2.2K 4 R549 *4.7K 4 NV_CLE [8] N.A at CPT EDS 0.7 H_SNB_IVB# [2]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V5S0 R283 *1K 4 ACZ_SYNC_R
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33_E ACZ_SDOOUT R259 *1K 4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R566 *1K 4 4/29 reserve. ICC_EN# [9]
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R550 *1K 4 PLL_ODVR_EN [9]
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R173 *1K 4 +3V

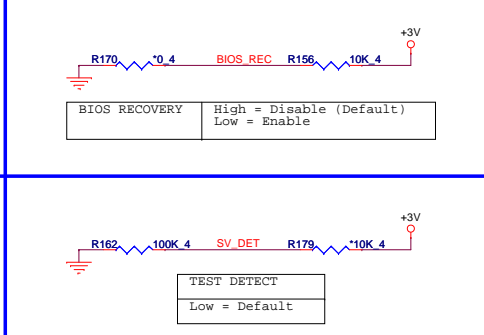
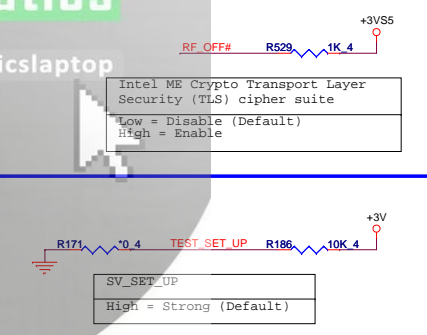
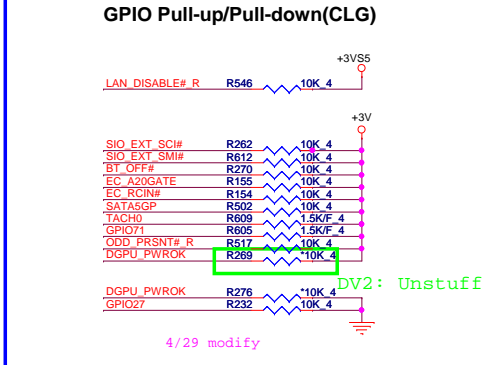
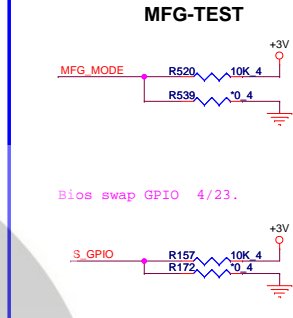
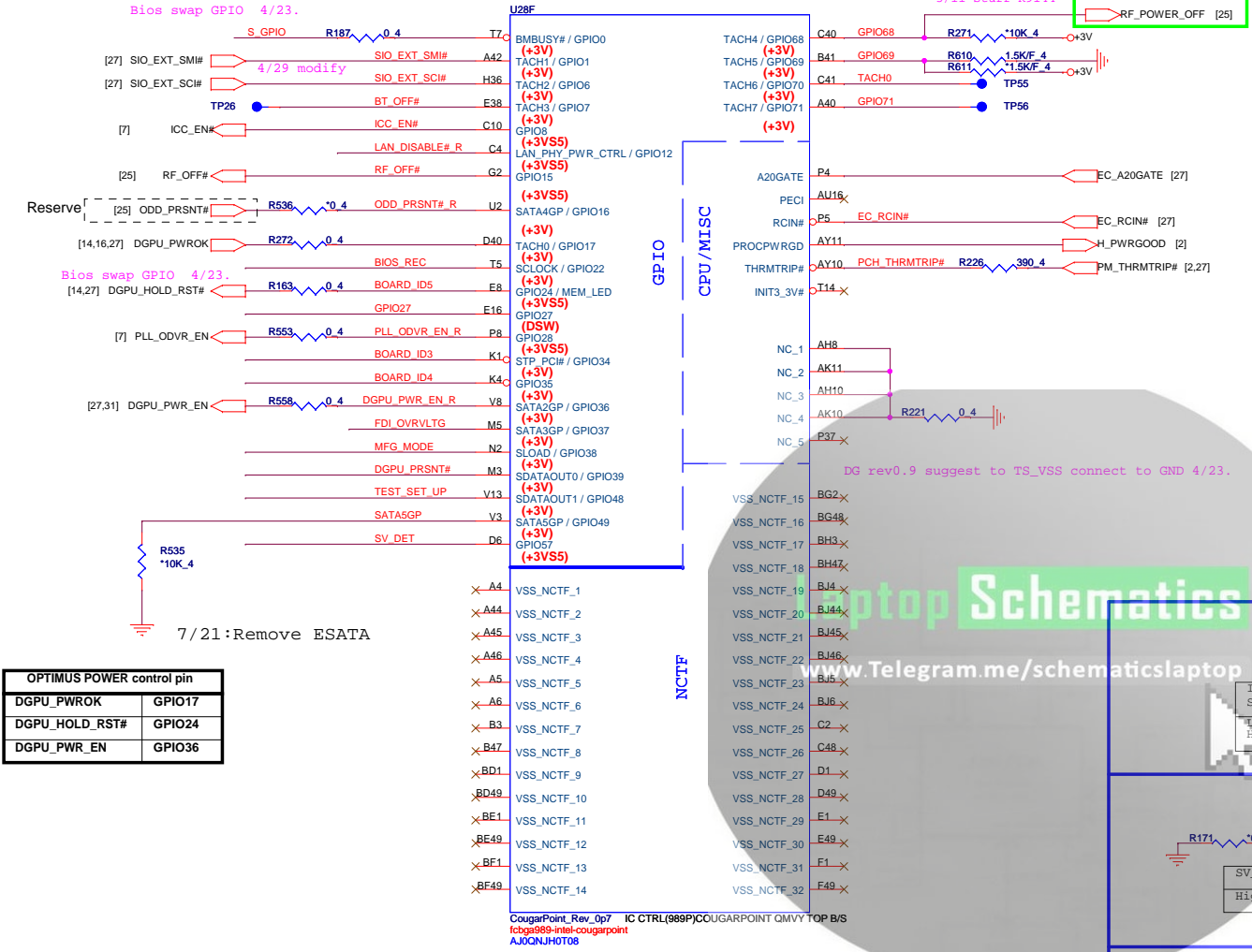
PROJECT : QLC
Quanta Computer Inc.
Arrandale+VGA

Size	Document Number	Rev
	PCH 2/6 (SATA/HDA/SPI)	1A

Date: Friday, November 26, 2010 Sheet 7 of 36

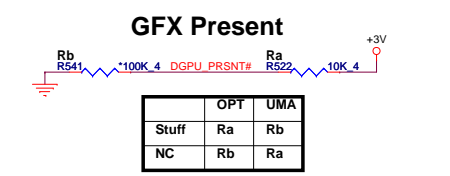
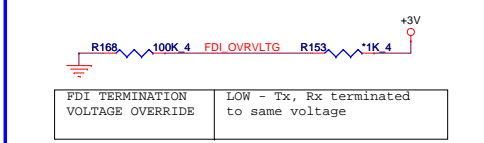
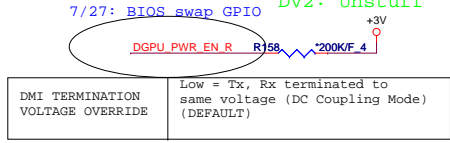
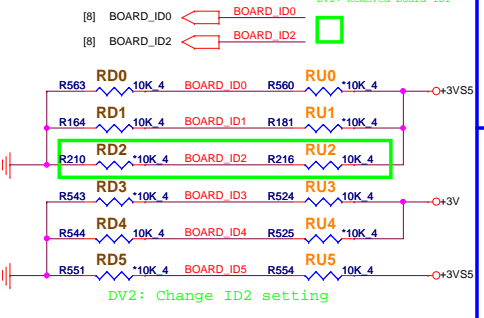


Cougar Point (GPIO,VSS_NCTF,RSVD)



BOARD ID SETTING

Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6
LG	0=LG 1=CB						
UMA/Dis.							
15.6"/ 14"			0=QLH/TWH 1=QLC/SWH				
MDC							
Dobly					0=NO 1=YES		
Optiums							

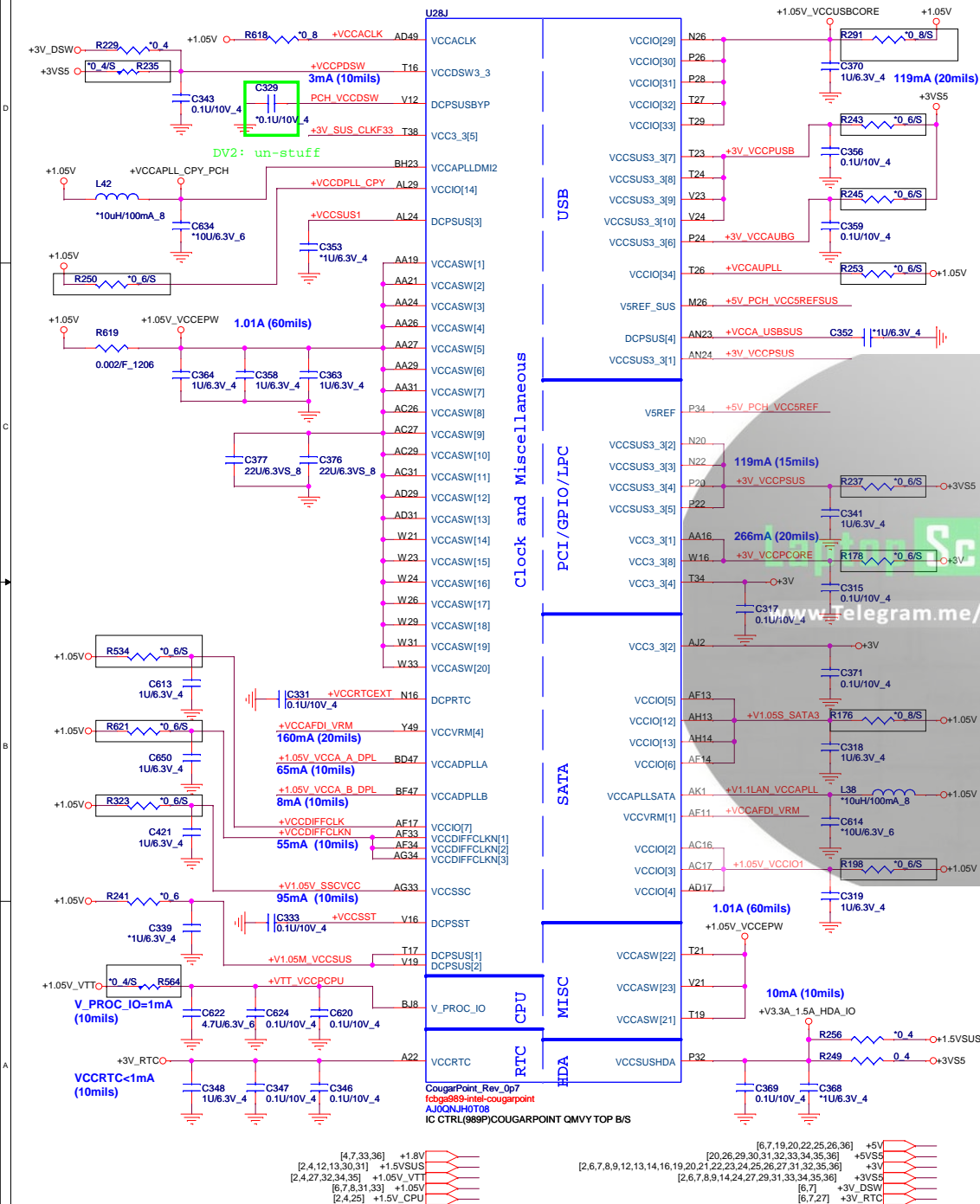


[2,6,7,8,10,12,13,14,16,19,20,21,22,23,24,25,26,27,31,32,35,36] +3V
[2,6,7,8,10,14,24,27,29,31,33,34,35,36] +3VSS

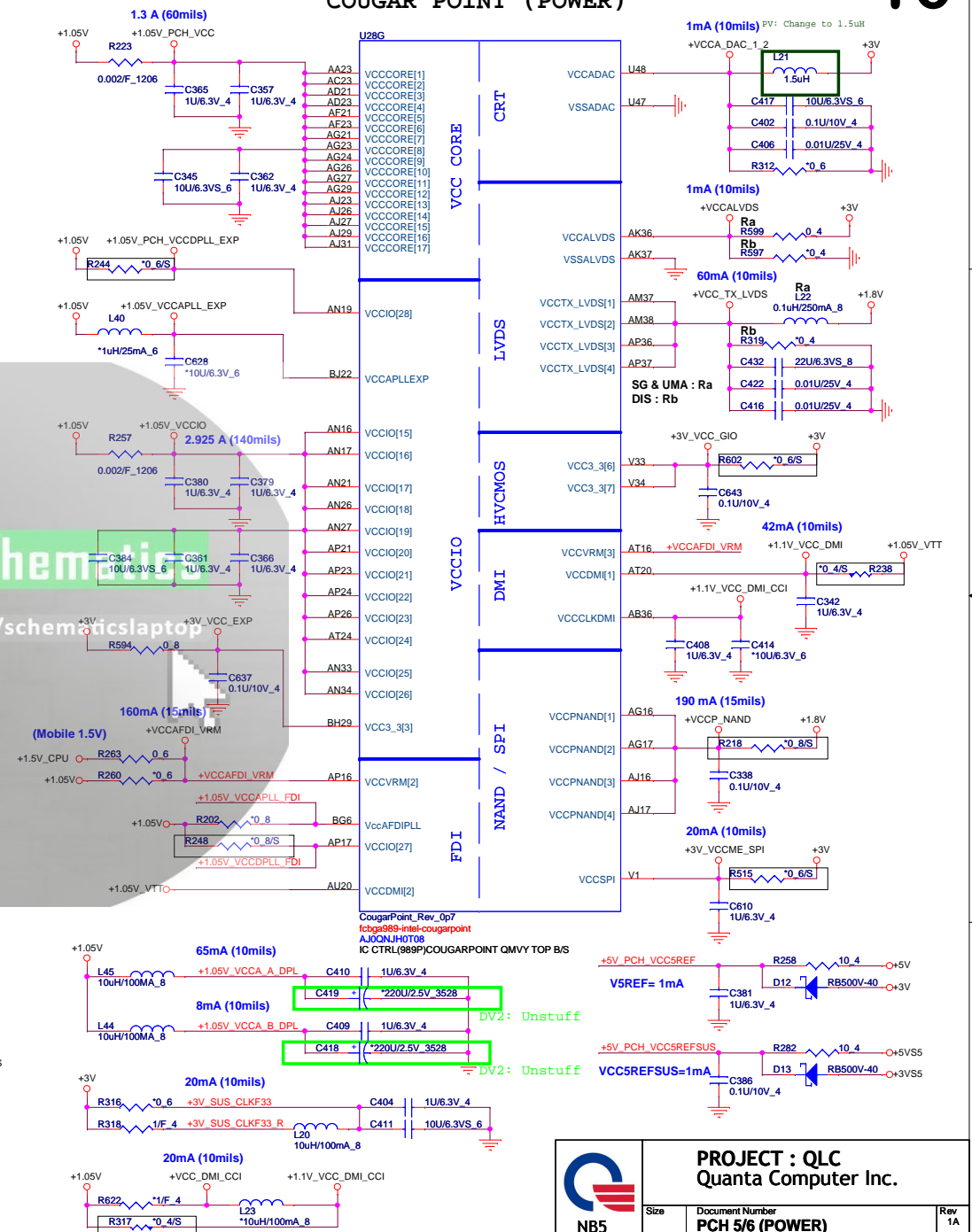
NB5	PROJECT : QLC Quanta Computer Inc. Arrandale+VGA			Rev 1A
	Size	Document Number PCH 4/6 (GPIO/MISC)	Date: Friday, November 26, 2010	

Sheet 9 of 36

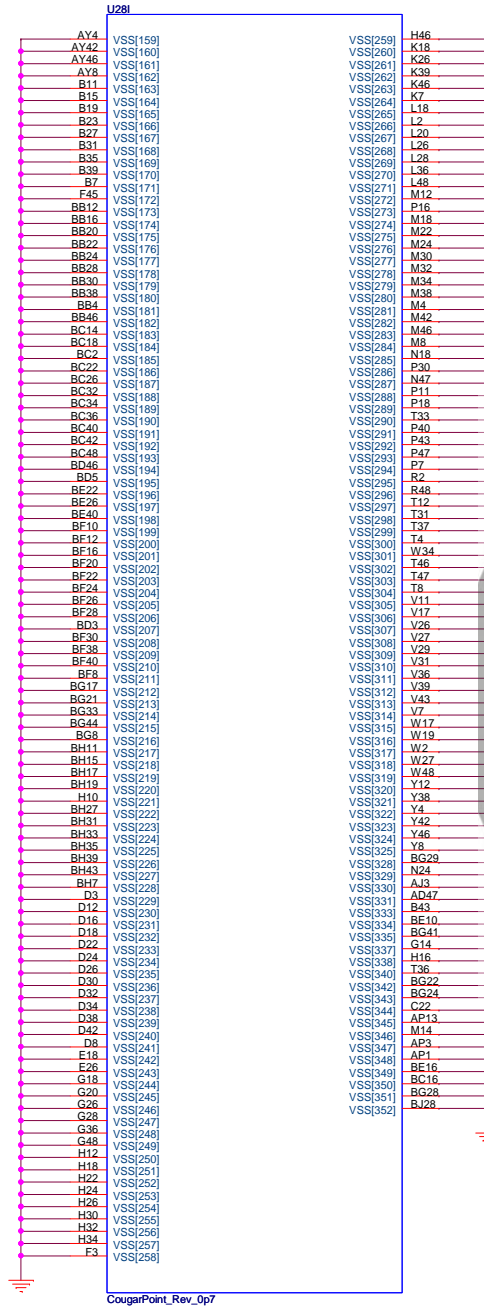
Cougar Point-M (POWER)



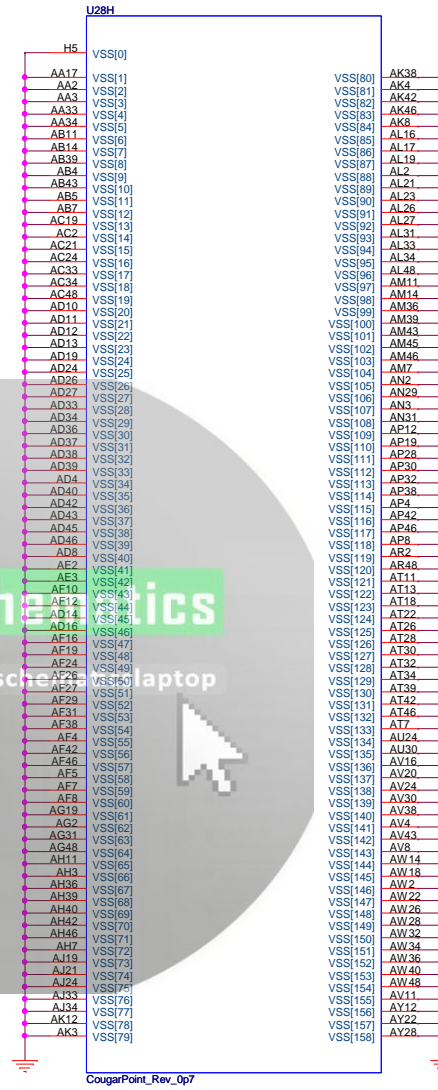
COUGAR POINT (POWER)



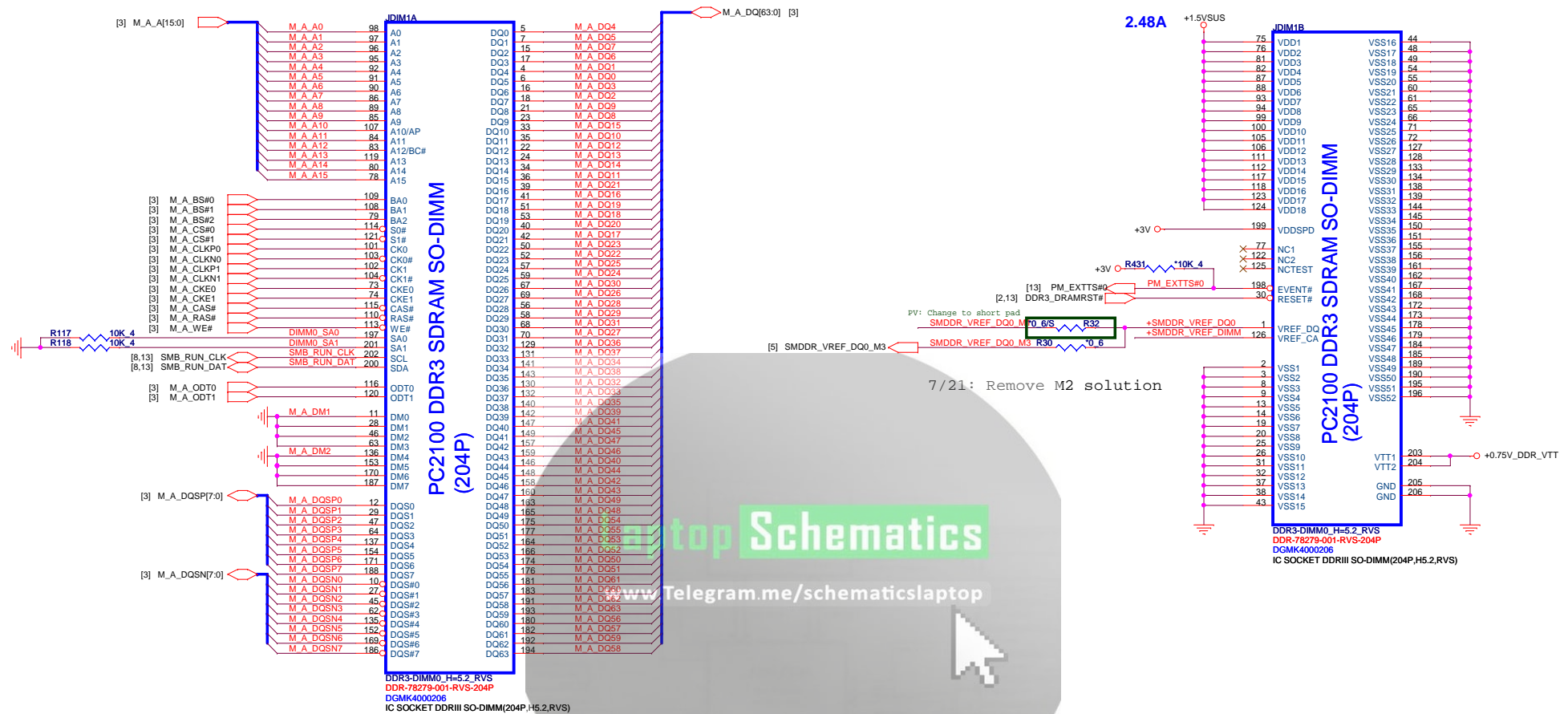
IBEX PEAK-M (GND)



IBEX PEAK-M (GND)



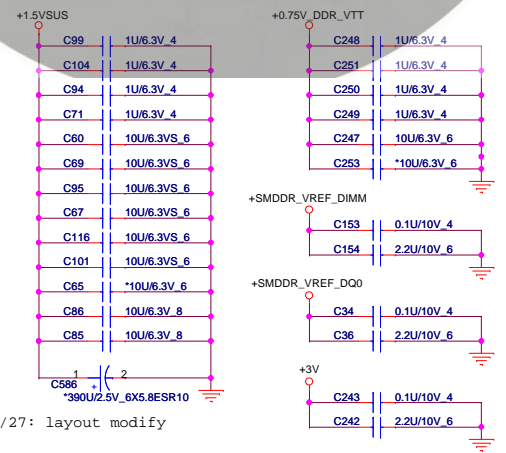
Laptop Schematics
www.Telegram.me/schematics_laptop



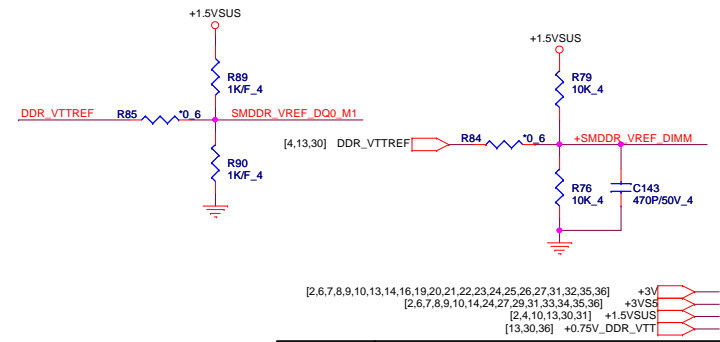
VREF DQ0 M2 Solution



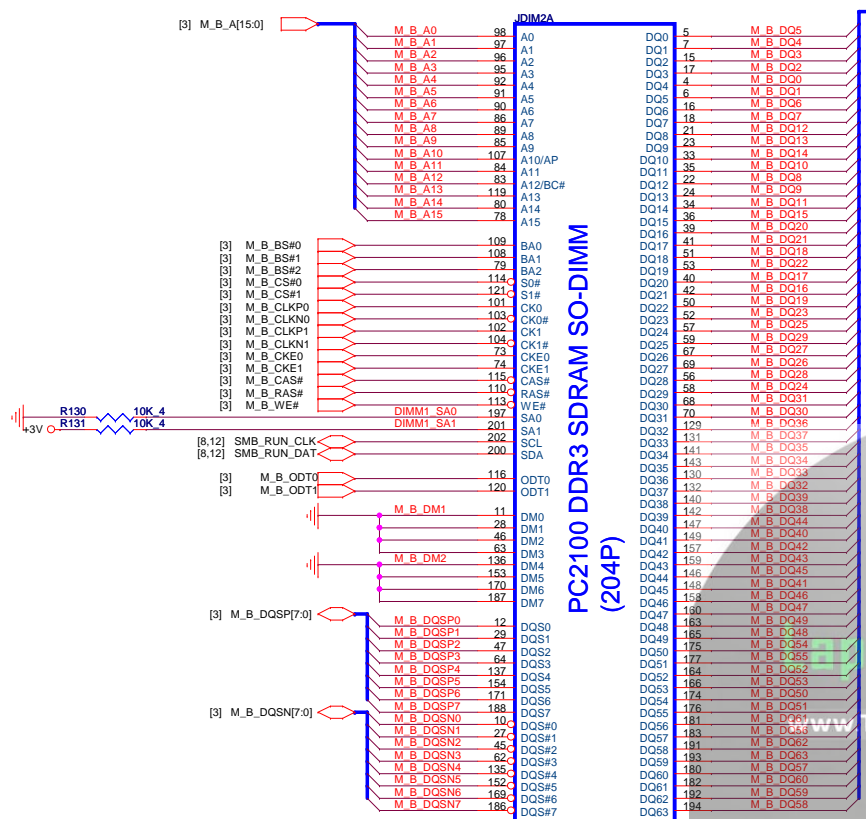
Place these Caps near So-Dimm0.



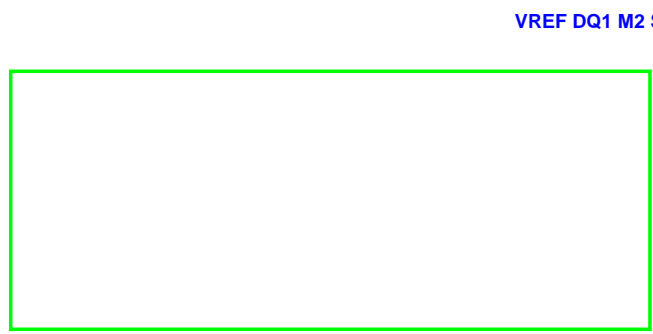
VREF DQ0 M1 Solution



4/29: reserve M2 solution
7/21: Remove M2 solution



DDR3-DIMM1_H=9.2_RVS
DDR-AS0A626-UARN-7F-204P
DGMK4000207
IC SOCKET DDRIII SO-DIMM(204P,H9.2,RVS)

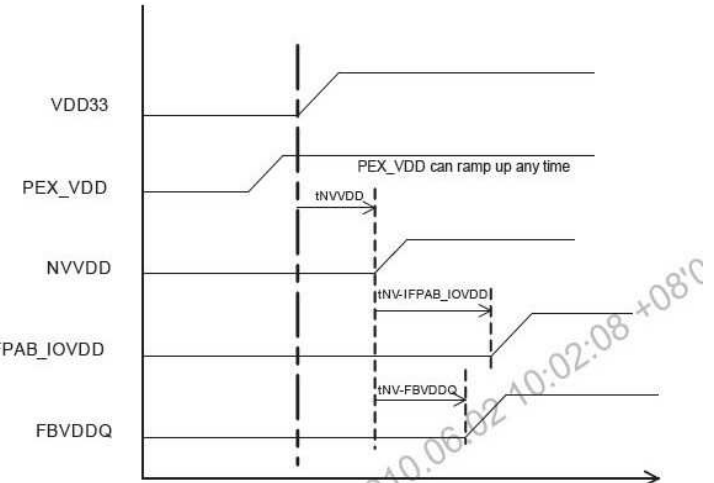


4/29 reserve M2 solution
7/21: Remove M2 solution

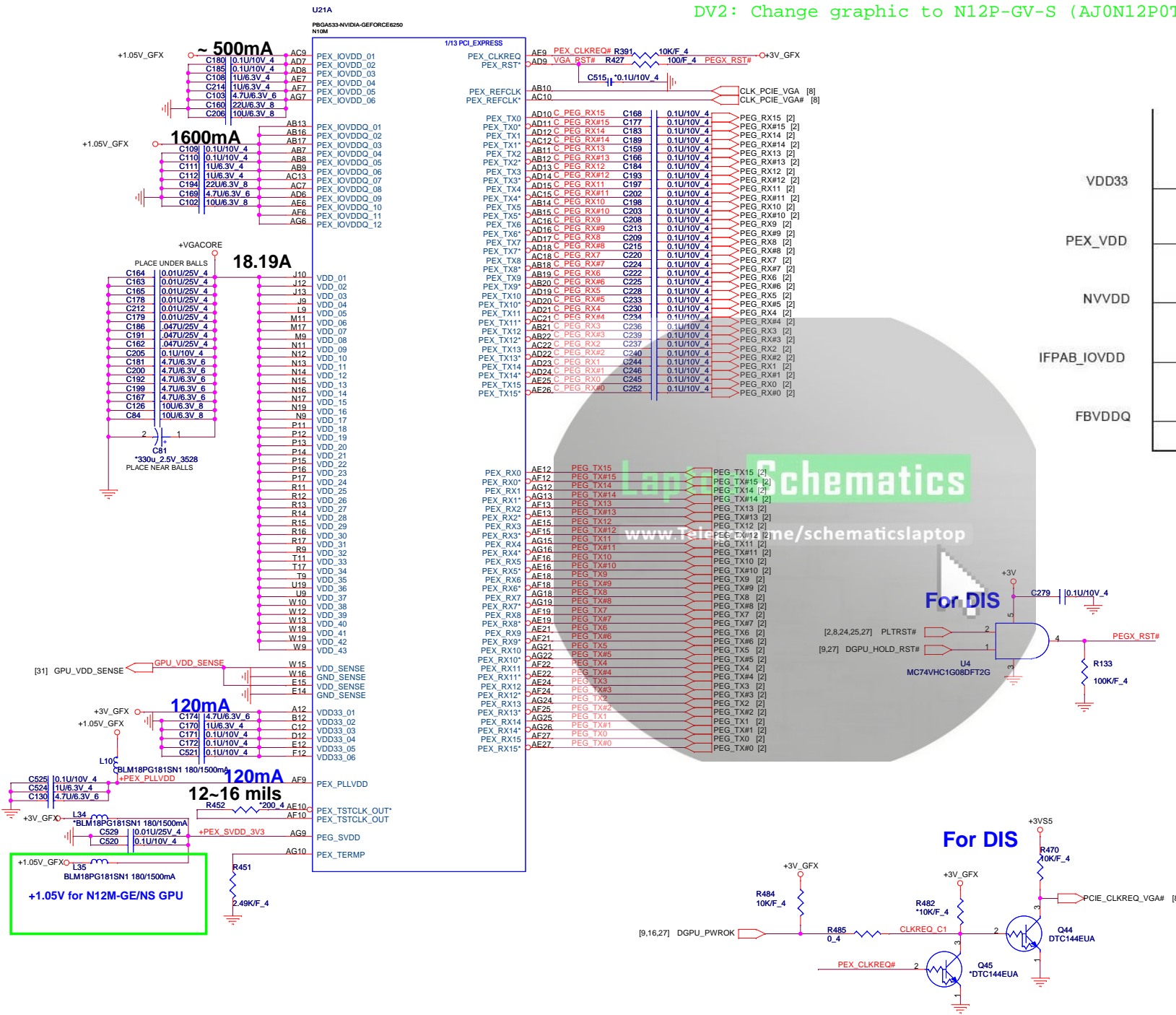
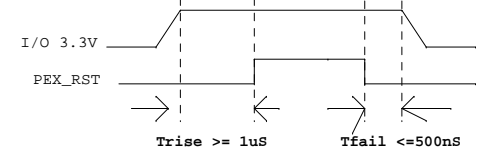


DV2: Change graphic to N12P-GV-S (AJ0N12P0T11)

power up sequence

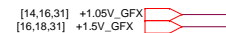


PEX_RST timing

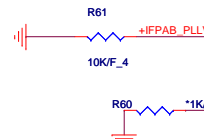


PROJECT : QLC
Quanta Computer Inc.

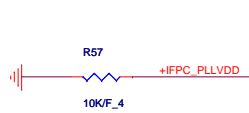
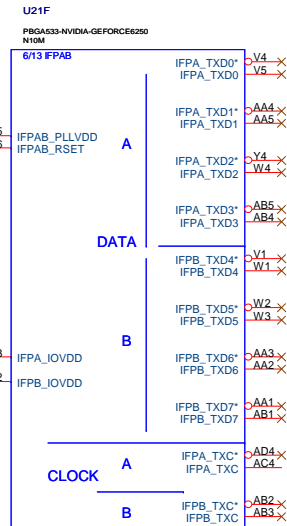
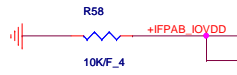
Size Custom	Document Number N11M-GE2(PCIE/F)	Rev ?
Date: Friday, November 26, 2010 Sheet 14 of 36		



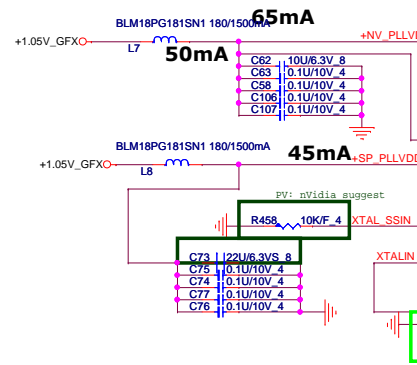
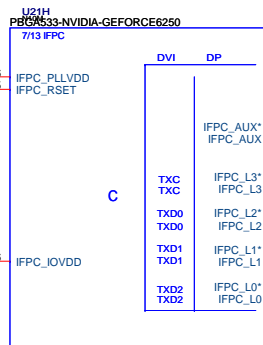
Optimus:
All unstuff , one Cap stuff 10K ohm



Optimus:
All unstuff , one Cap stuff 10K ohm



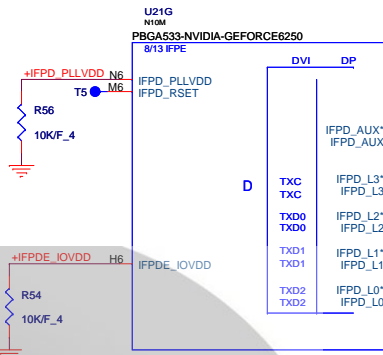
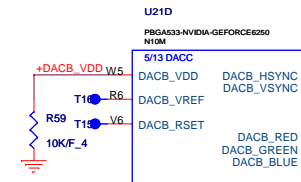
nVIDIA comment 8/18



DV2: Change to 27pF

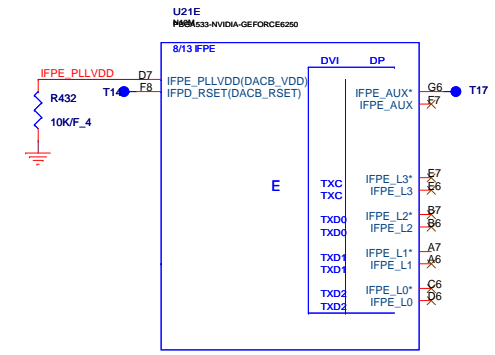
Laptop Schematics
www.Telegram.me/schematics1608

DV2: Removed 27MHz

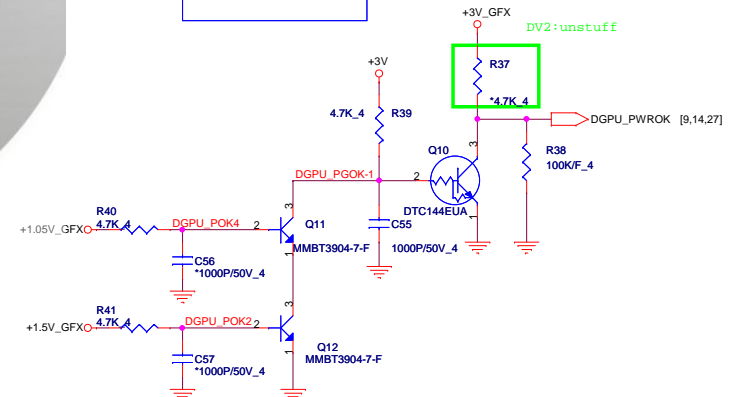
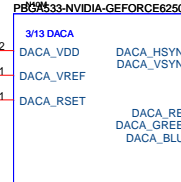


Optimus:
All unstuff , one Cap stuff 10K ohm

nVIDIA comment 8/18



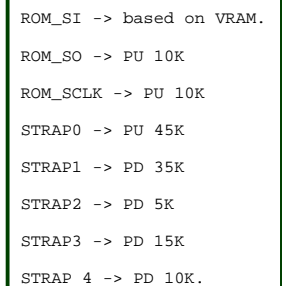
Optimus:
All unstuff , one Cap stuff 10K ohm



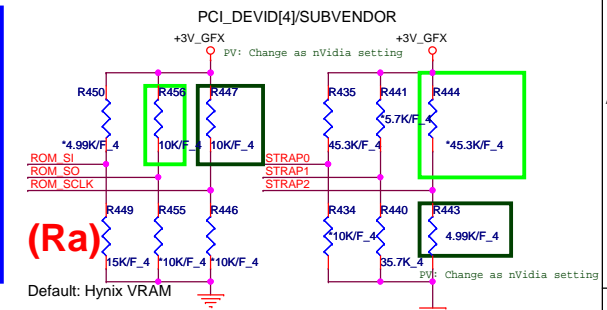
PROJECT : QLC
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N11M-GE2(DISPLAY)	?
Date: Friday, November 26, 2010	Sheet 16 of 36	

[2,6,7,8,9,10,12,13,14,19,20,21,22,23,24,25,26,27,31,32,35,36] +3V
[14,17,19,31] +3V_GFX
[14,15,31] +1.05V_GFX

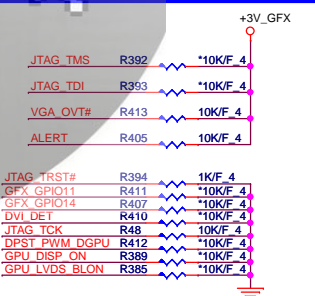
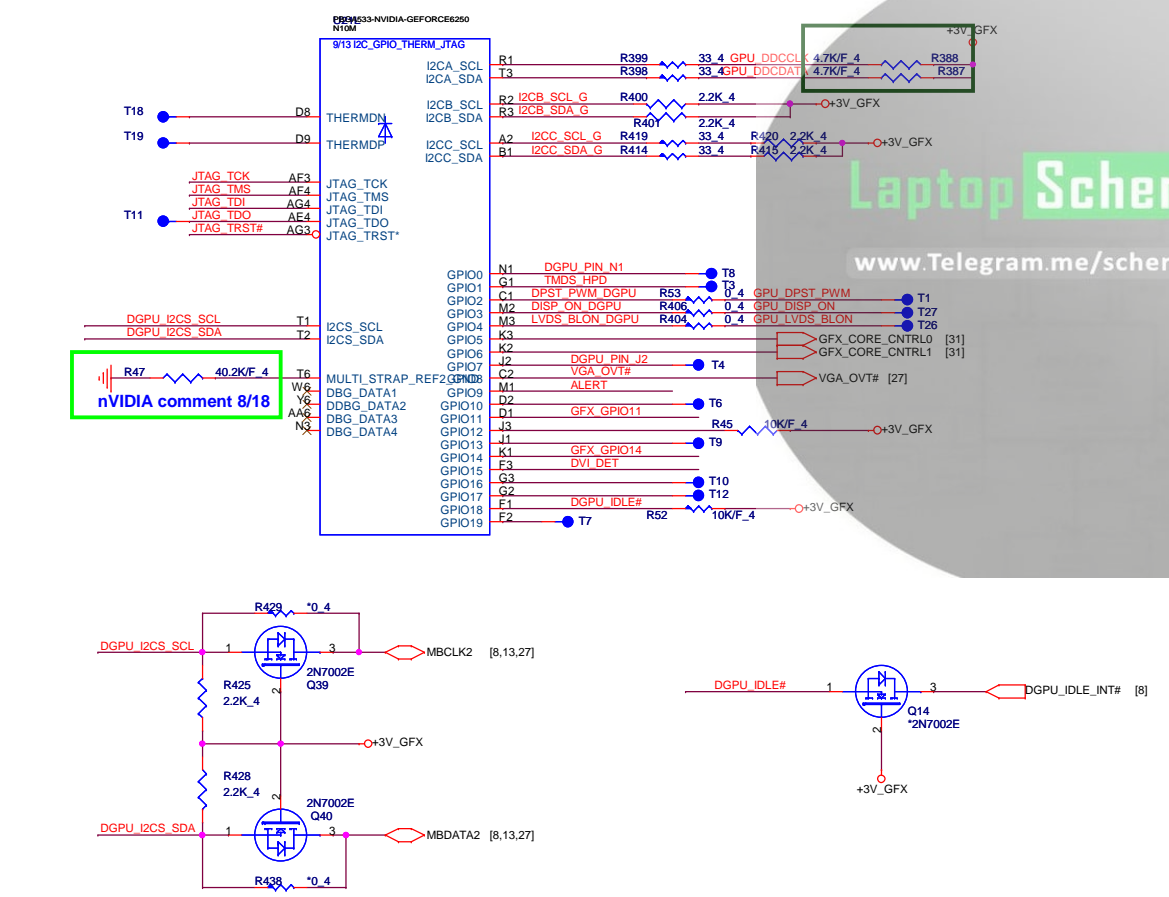


Logical Strap Bit Mapping		
	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVICE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix		PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung		PD 20K
0110	DDR3 128Mx16x4, 128bit, 1GB,800MHz	Hynix		PD 35K
0111	DDR3 128Mx16x4, 128bit, 1GB,800MHz	Samsung		PD 45K
XXXX				
XXXX				



GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVD VDD VID0
6	OUT	N/A	NVVD VDD VID1
7	OUT	N/A	NVVD VDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	Memory VREF SELECT
11	I/O	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	THERM_LOAD_STEP_DOWN
14	OUT	N/A	THERM_LOAD_STEP_UP

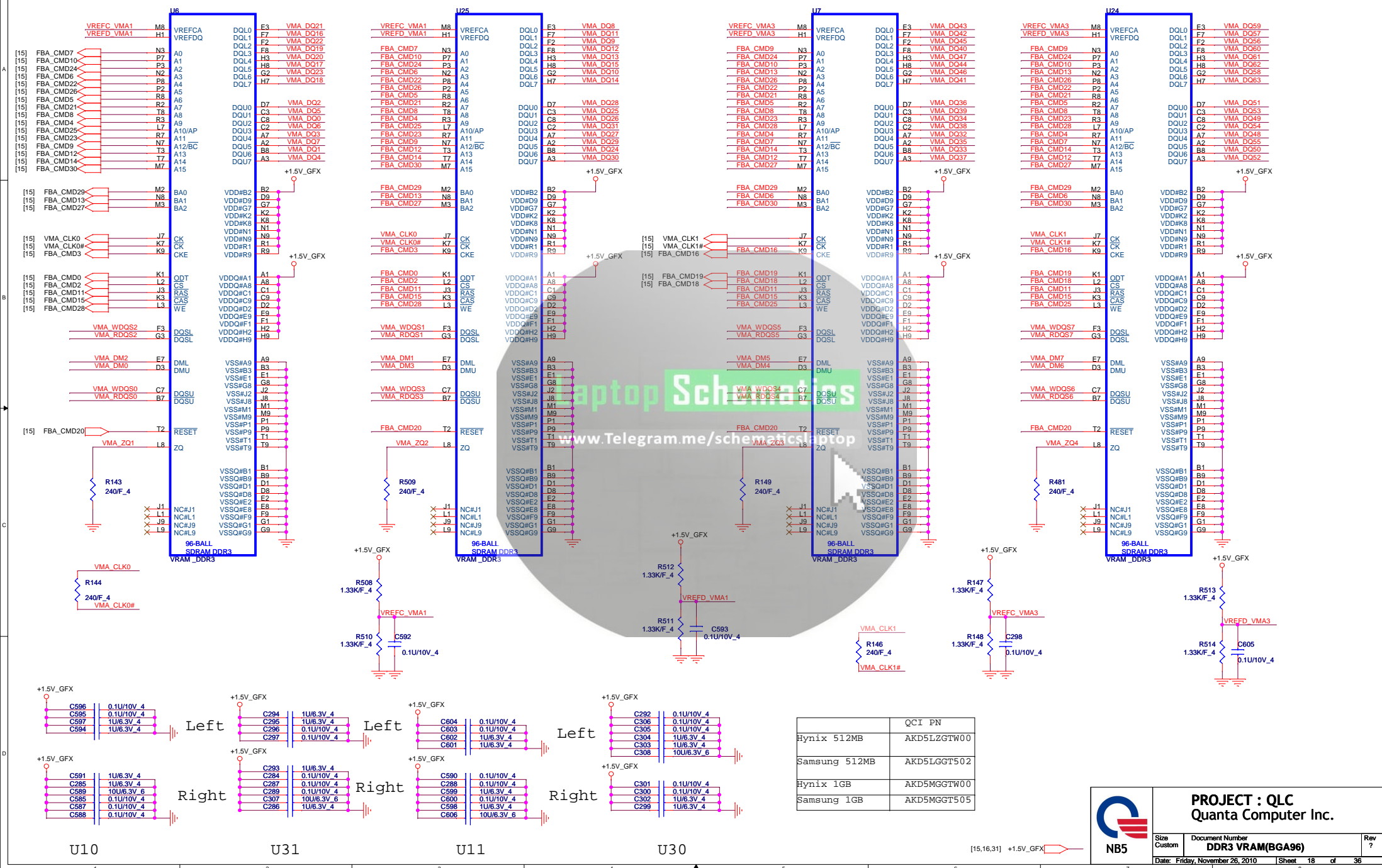
CHANNEL A: 256MB/512MB DDR3

[15] VMA_DQ[63..0]

[15] VMA_DM[7..0]

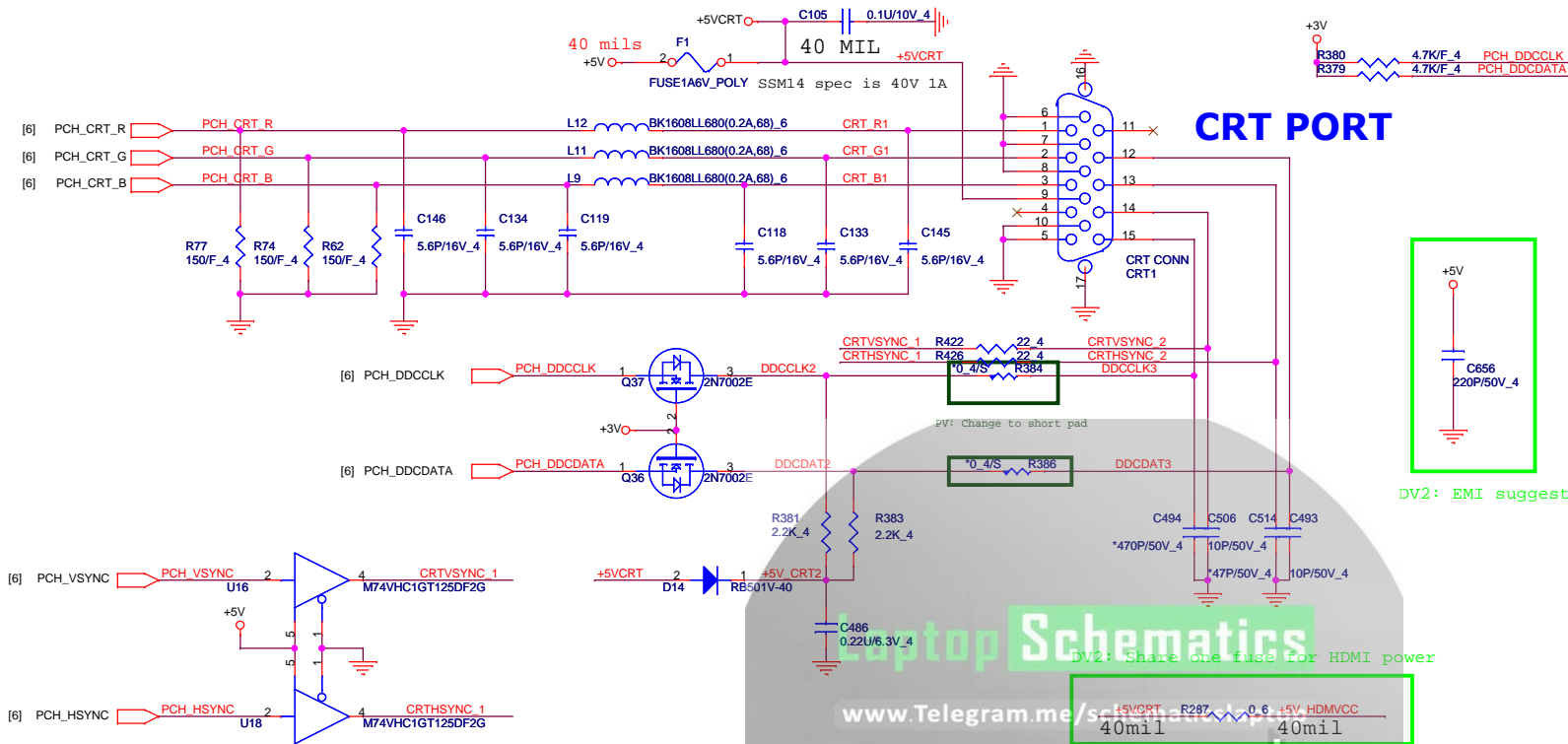
[15] VMA_WDQS[7..0]

[15] VMA_RDQS[7..0]

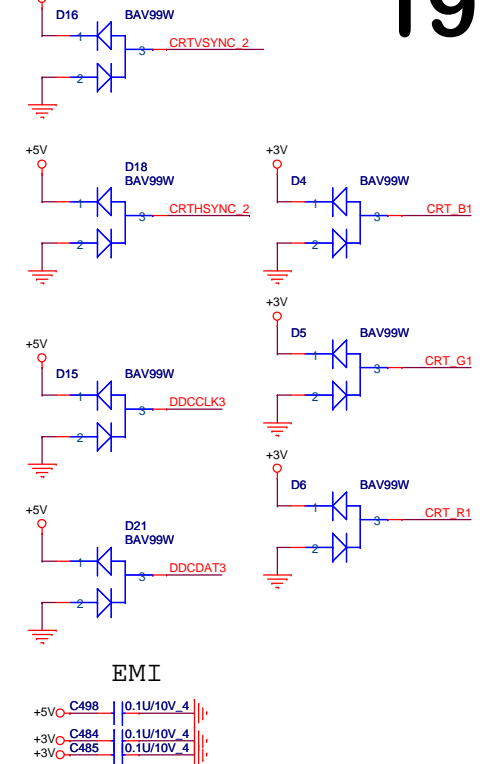


	QCI PN
Hynix 512MB	AKD5LZGTW0
Samsung 512MB	AKD5LGGT50
Hynix 1GB	AKD5MGGTW0
Samsung 1GB	AKD5MGGT50

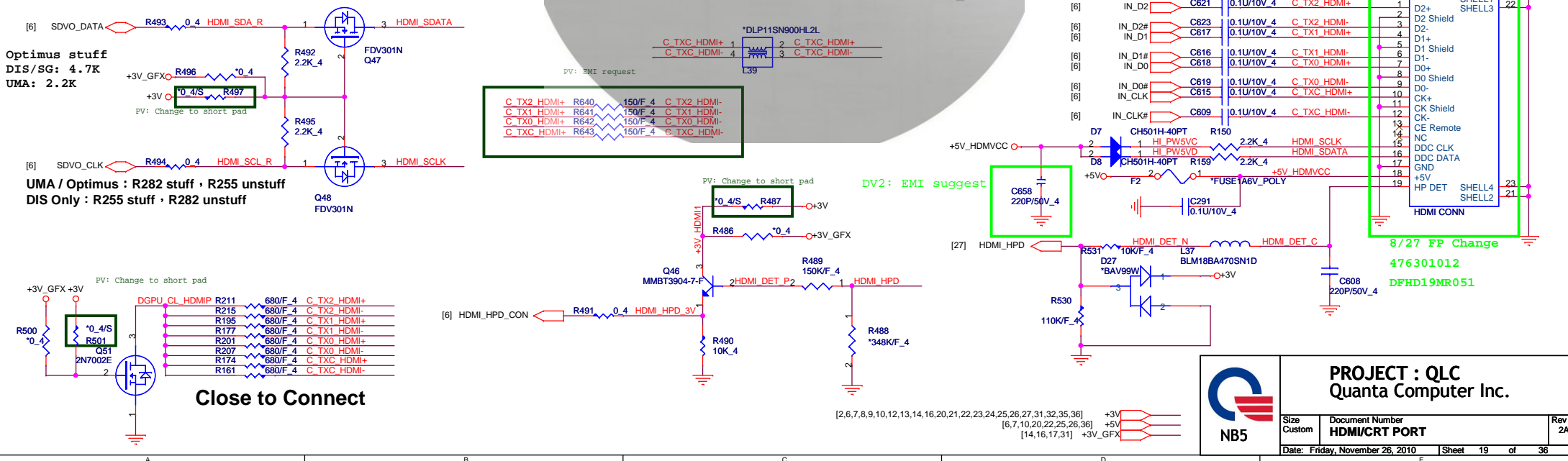
Close to Connect

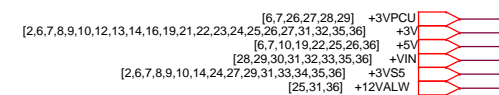
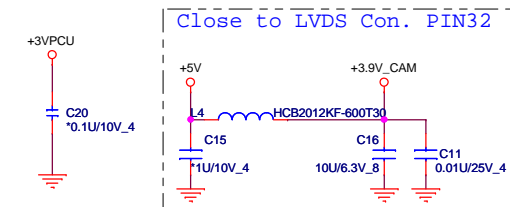
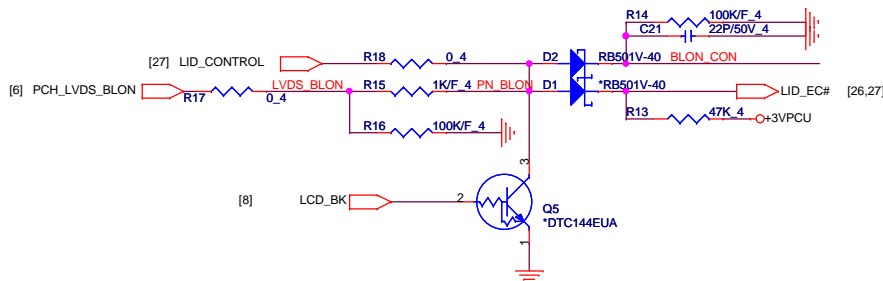
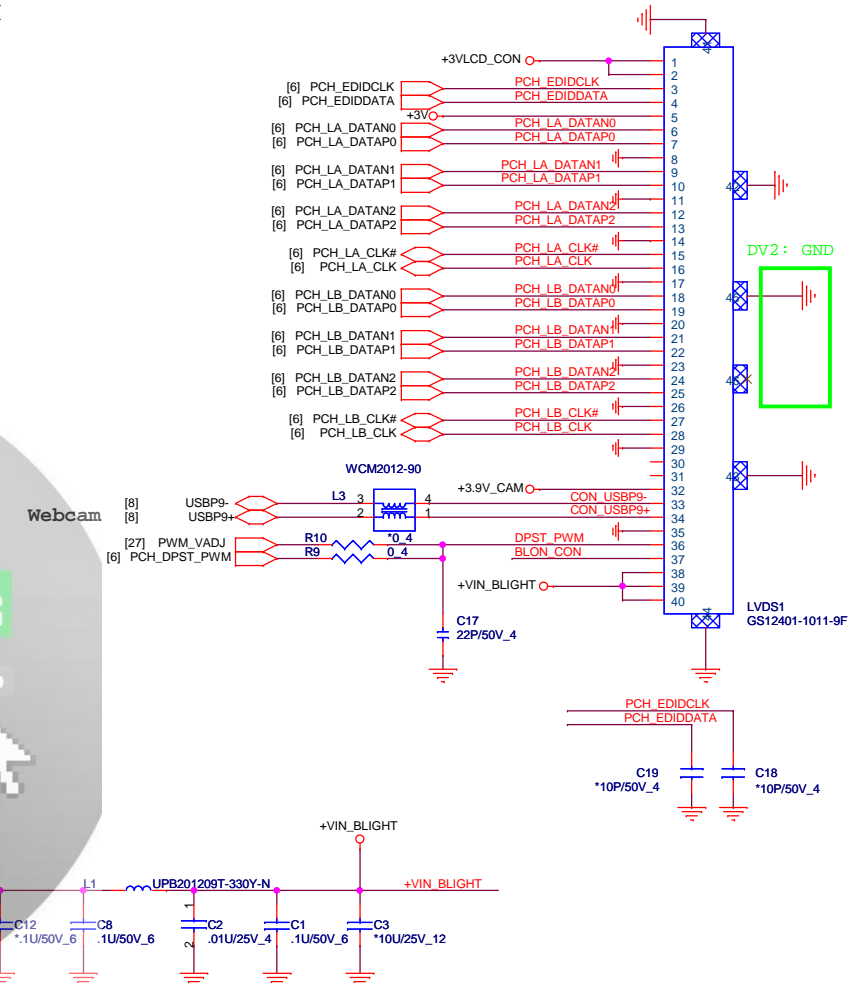
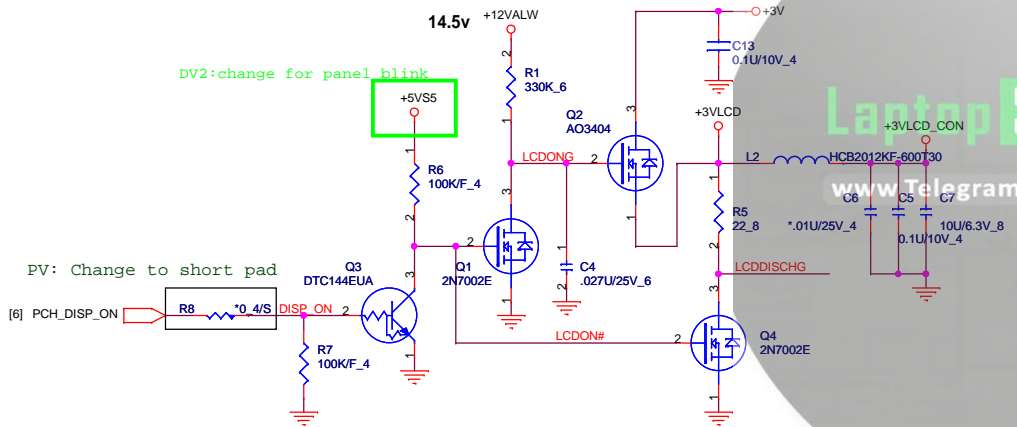
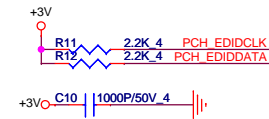


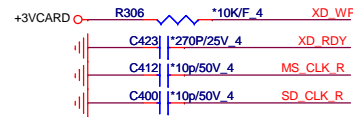
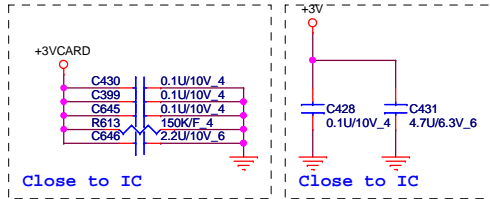
ESD PROTECTION



HDMI PORT

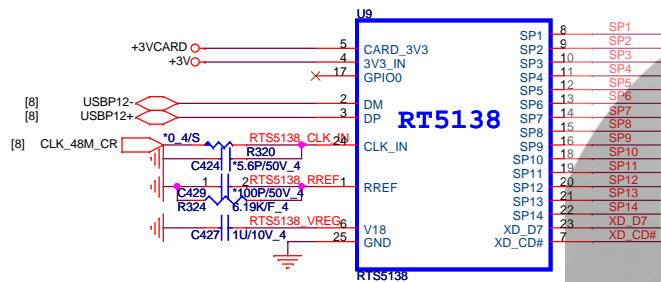






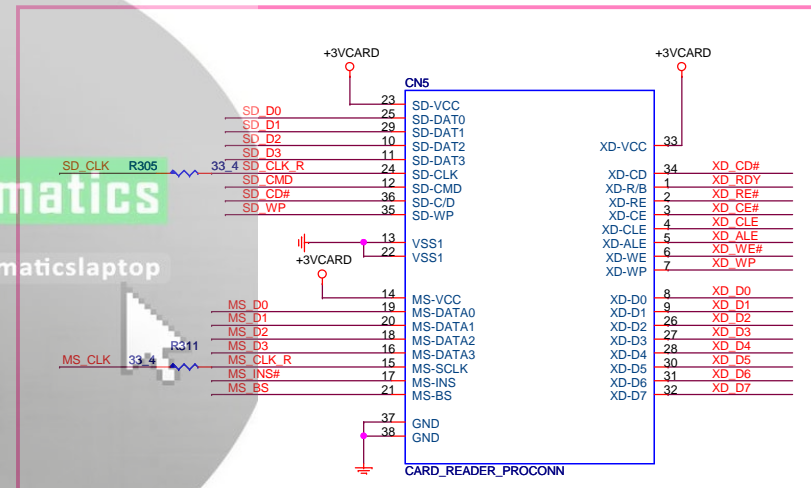
SP1	XD CD#	SD WP	MS CLK
SP2	XD RDY	SD WP	MS CLK
SP3	XD RE#	SD D1	MS INS#
SP4	XD CE#	SD D0	
SP5	XD ALE	SD D7	MS D3
SP6	XD WE#	SD CD#	
SP7	XD WP	SD D6	
SP8	XD D0	SD CLK	MS D2
SP9	XD D1	SD D5	MS D0
SP10	XD D2	SD CMD	
SP11	XD D3	SD D4	
SP12	XD D4	SD D3	MS D1
SP13	XD D5	SD D2	
SP14	XD D6		MS BS
	XD D7		

Share Pin

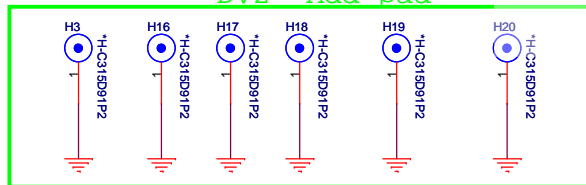


Laptop Schematics

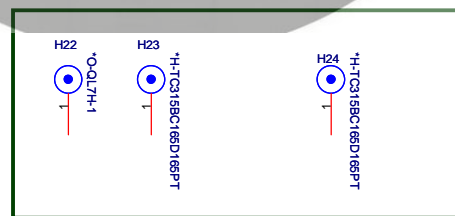
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DV2: Add pad

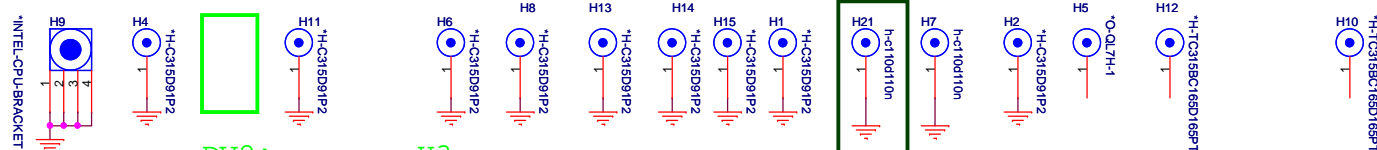


PV: Add as ME request

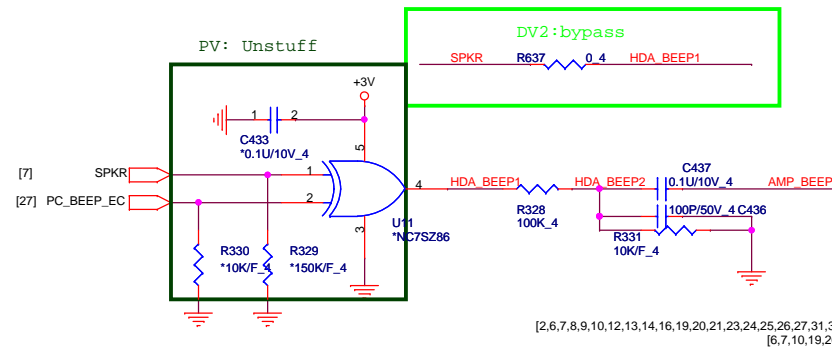
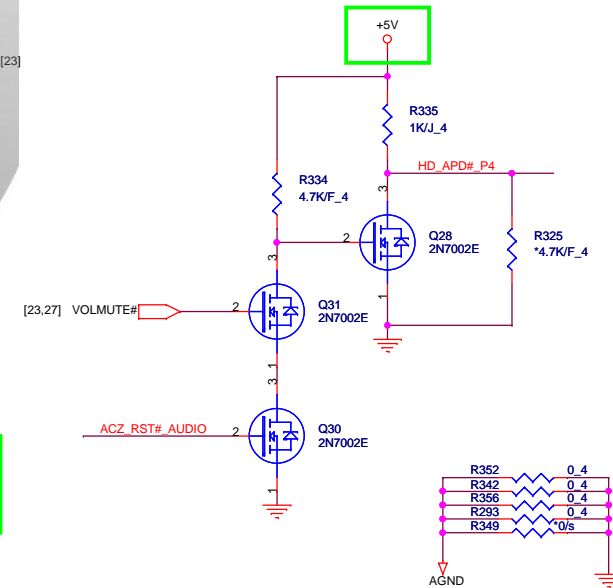
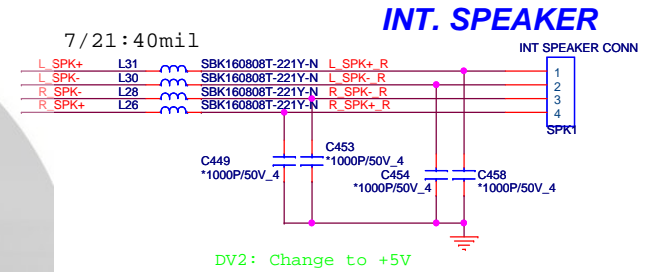
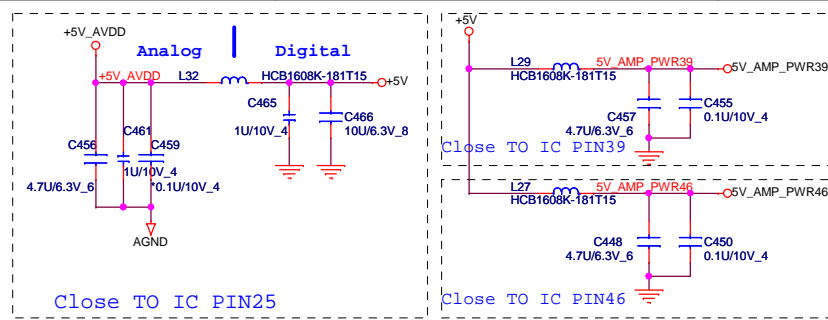
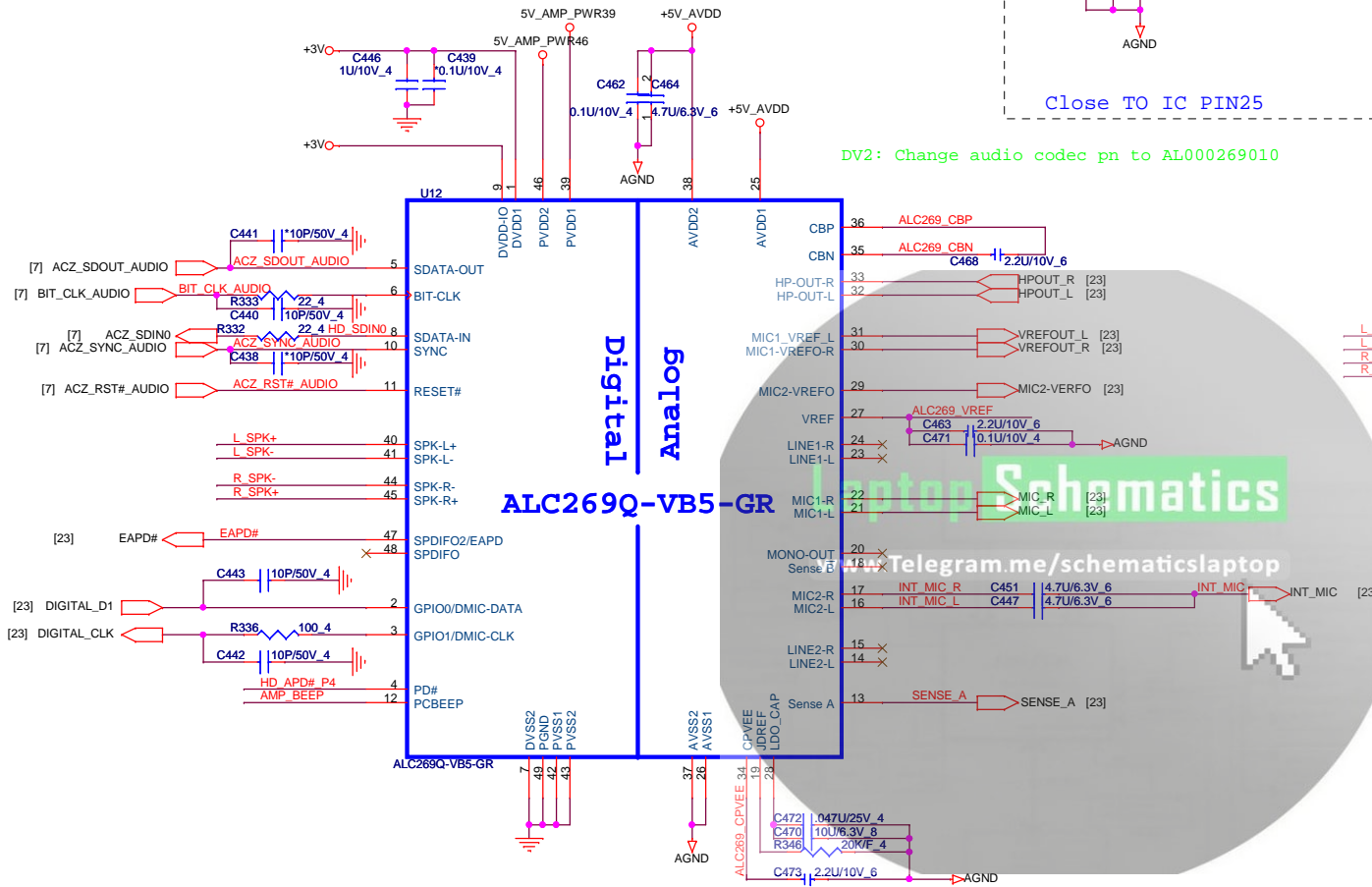


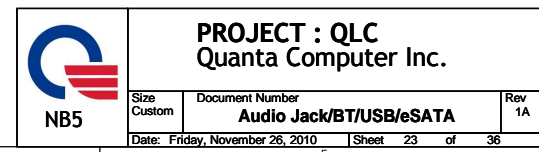
7/27: Change CPU BKT to INTEL-CPU-BKT2

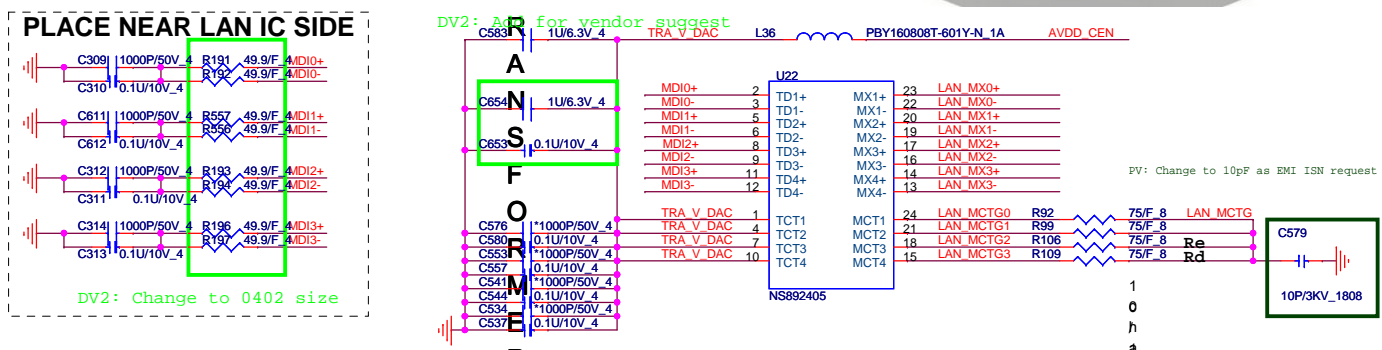
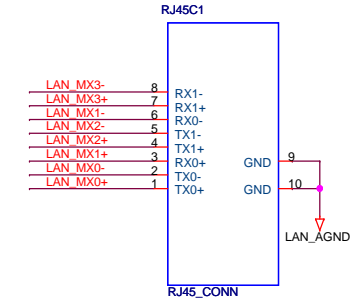
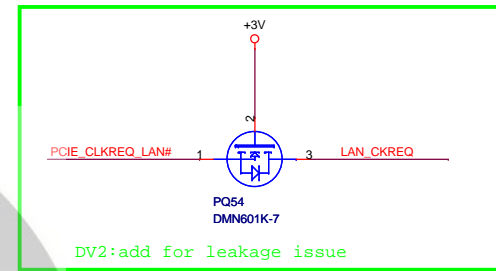
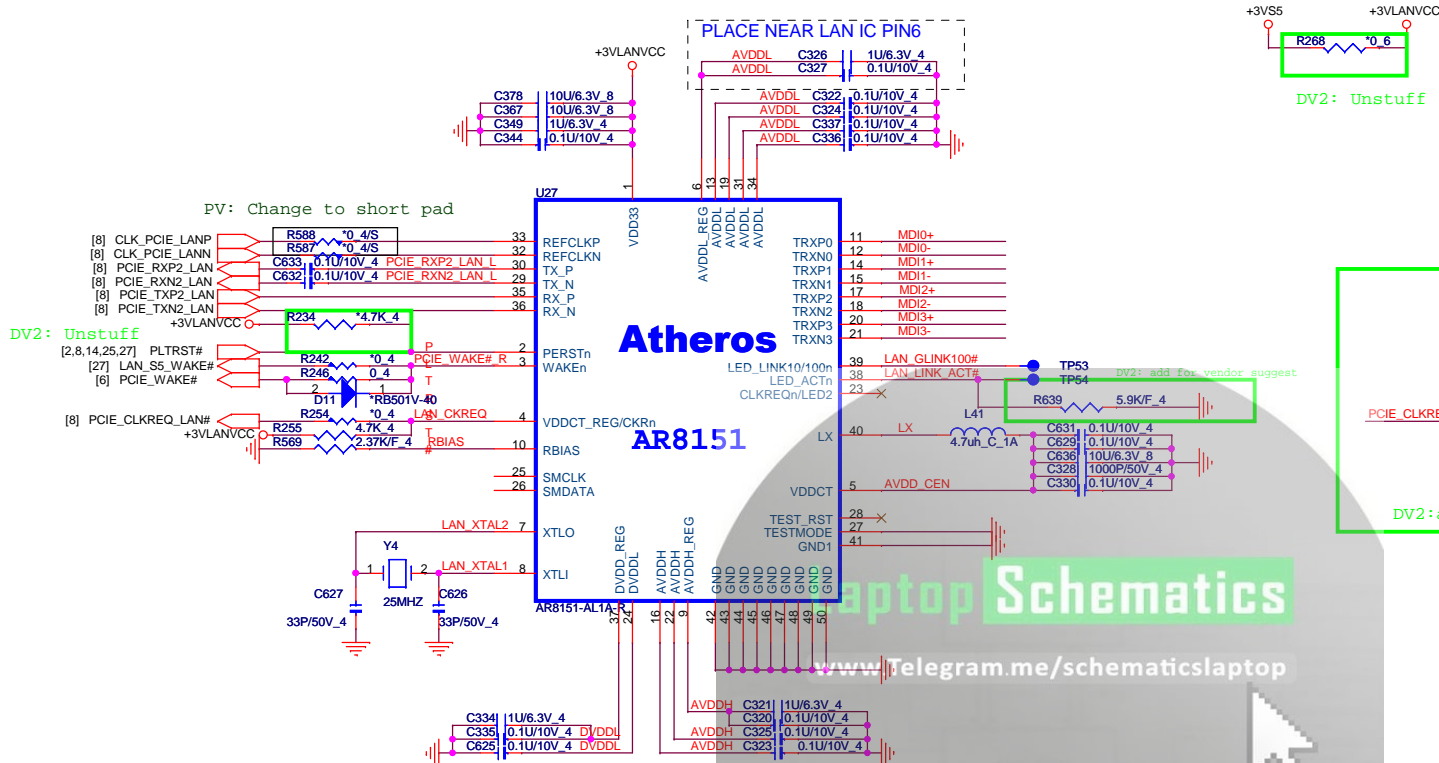
8/3: Change back INTEL-CPU-BRACKET



DV2: remove H3

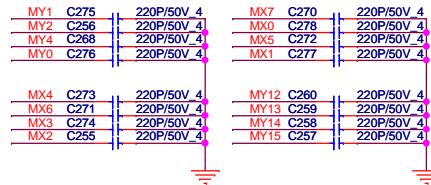
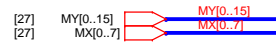




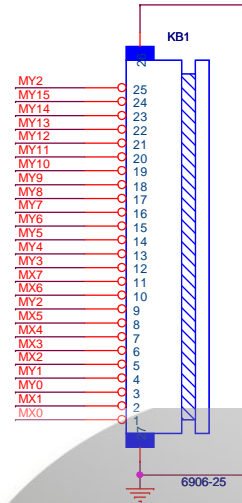
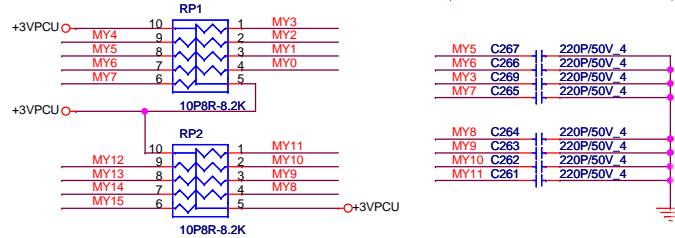


D3A: only UMA sku support 1G, If support 10/100 in UMA SKU, R55, R56 change to 0-ohm

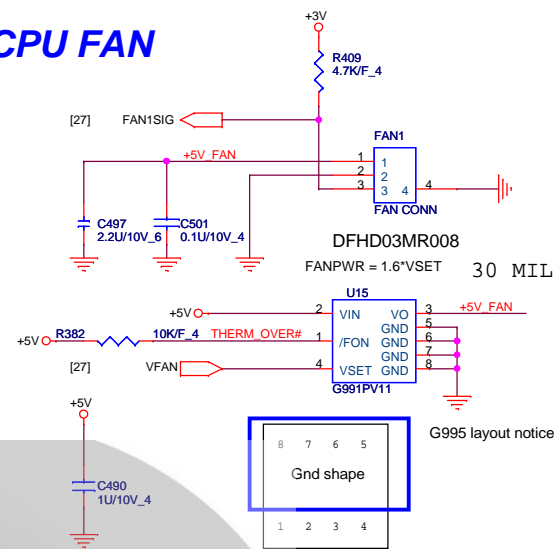
KEYBOARD Con.



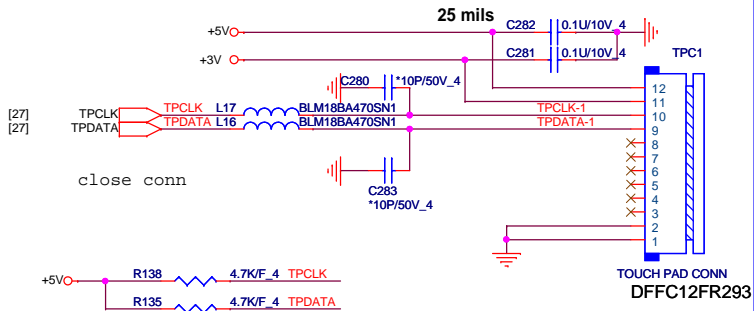
KEYBOARD PULL-UP



CPU FAN

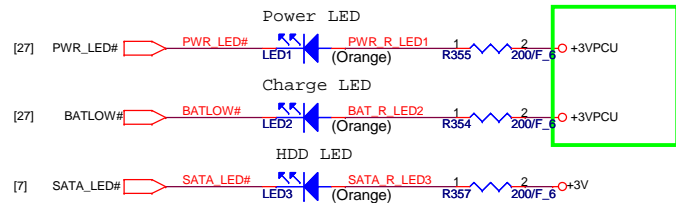


TOUCH PAD CONNECTOR



LED

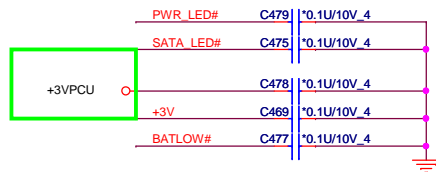
10 mils (250mA)



Left ----> Right

Power LED / Charge LED / HDD LED

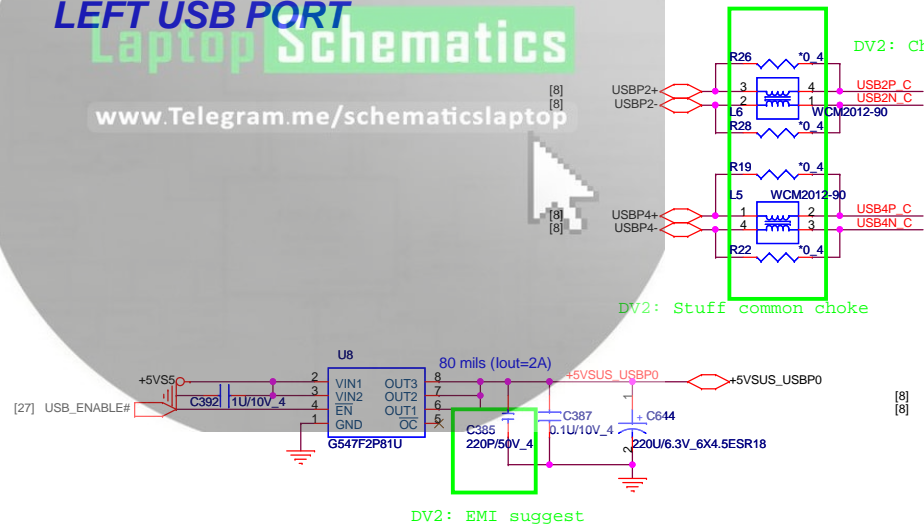
DV2: Change from +3VPCU_EC to +3VPCU



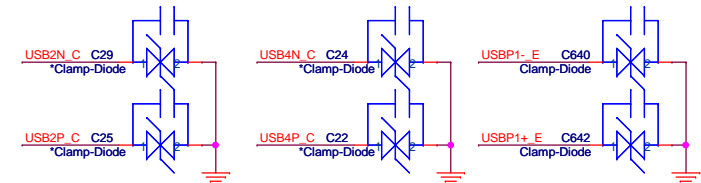
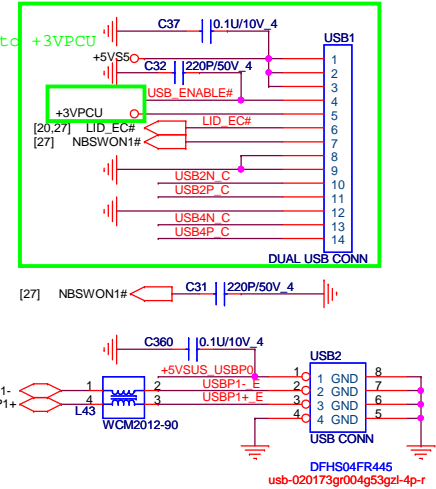
LEFT USB PORT

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TO USB BOARD conn



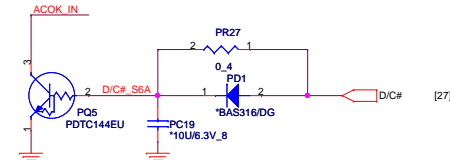
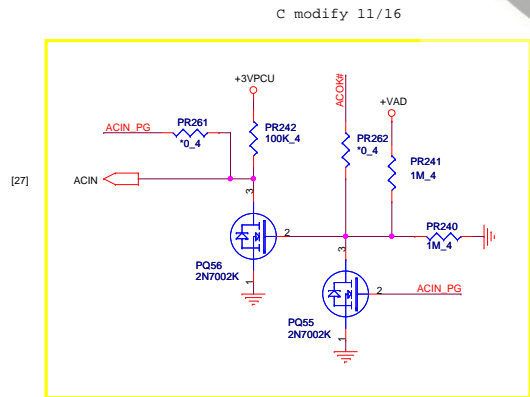
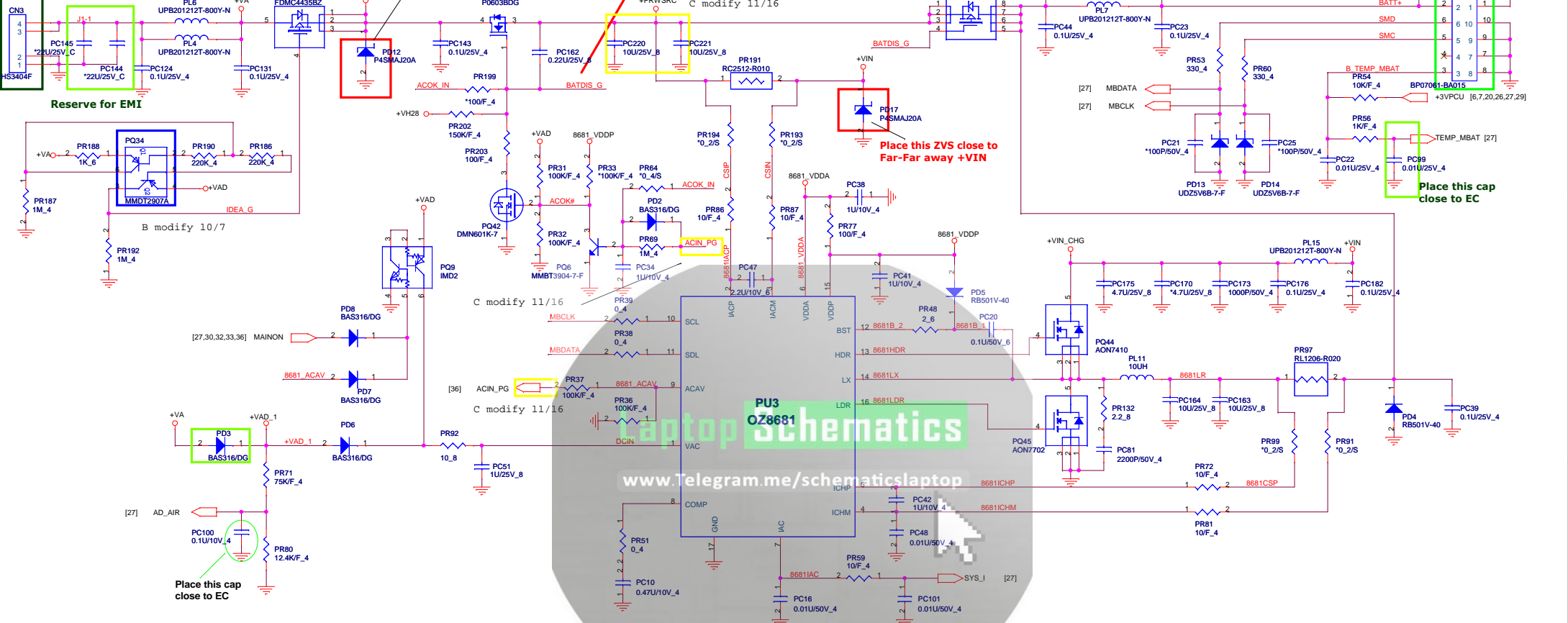
PROJECT : QLC
Quanta Computer Inc.

[2,6,7,8,9,10,12,13,14,16,19,20,21,22,23,24,25,27,31,32,35,36] [6,7,10,19,20,22,25,36] +5V
[6,7,20,27,28,29] +3V
+3VPCU

Size Custom	Document Number KB/FAN/LED/TP/ODD/HDD	Rev 1A
Date: Friday, November 26, 2010		Sheet 26 of 36

PV1: change CN3 footprint to 87299-0441-4P-L

**TOP DC_JACK
65W/90W**

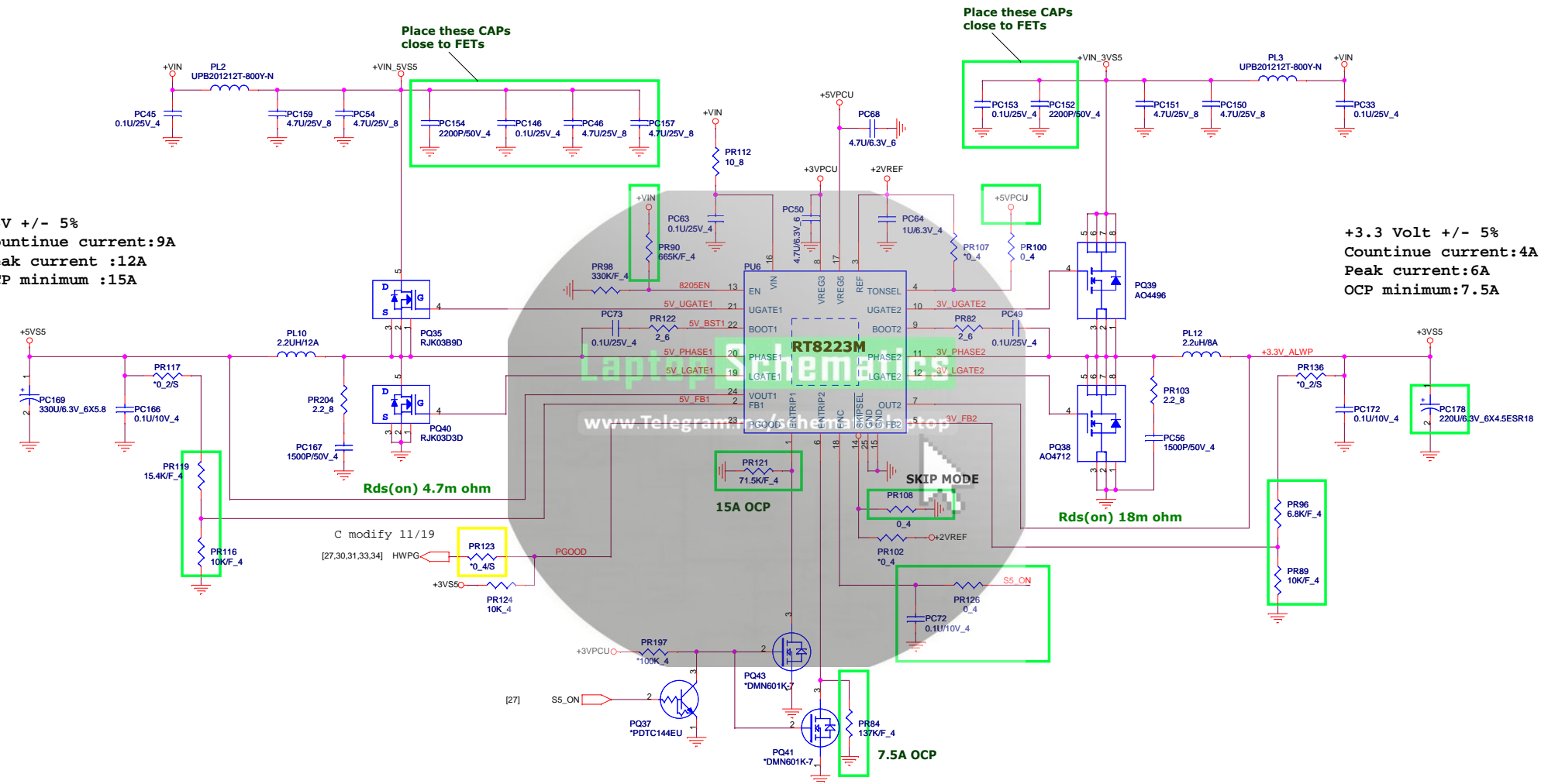


- [36] +BATCHG
- [36] +VAD_1
- [36] +VH28
- [36] +VA

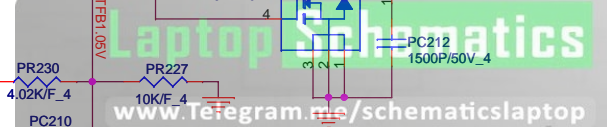
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

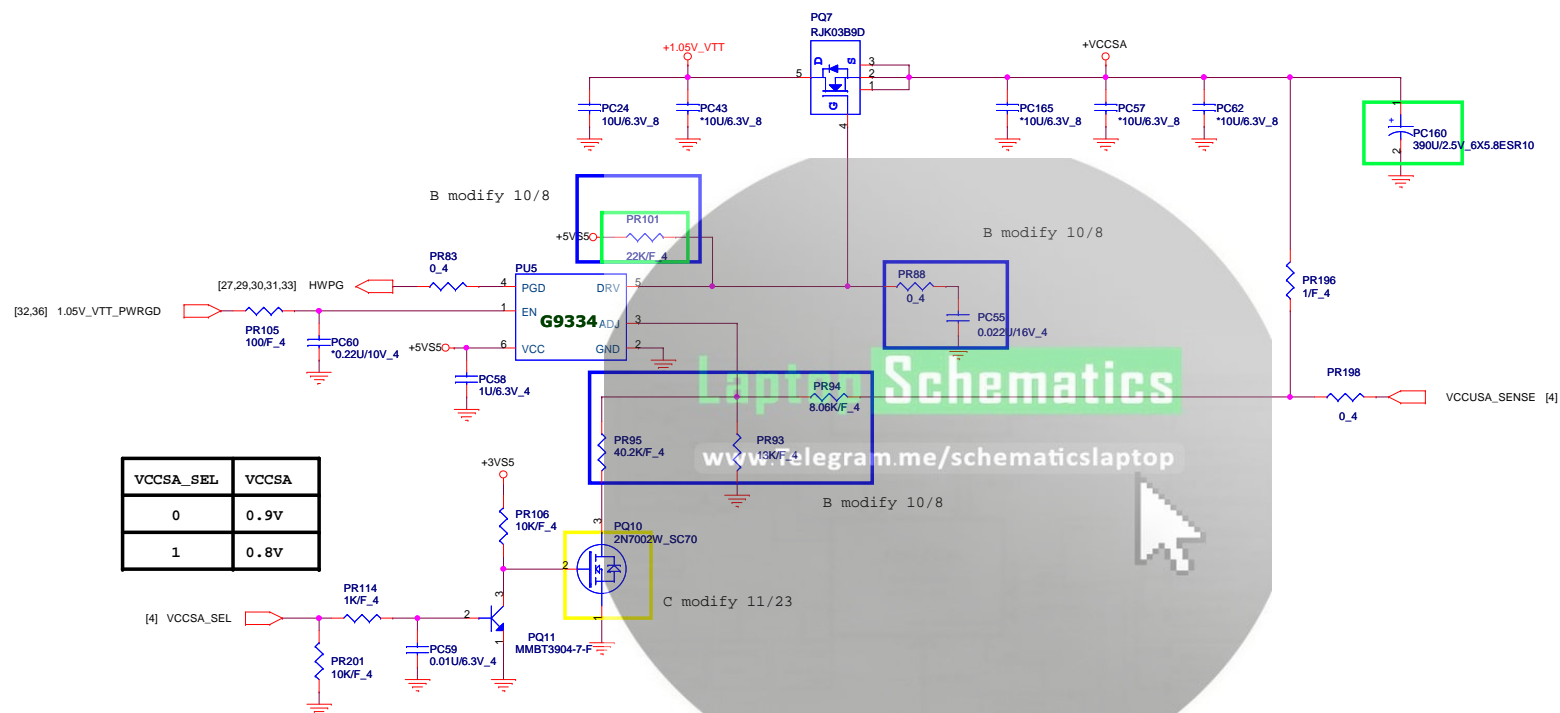
+5V +/- 5%
 Countinue current:9A
 Peak current :12A
 OCP minimum :15A

+3.3 Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A

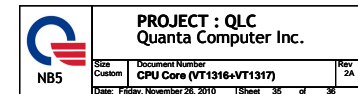








43/111



A --> B

1. Change R101 connection from PM_DRAM_PWRGD_R to PM_DRAM_PWRGD_C
2. Add R632 as Intel suggest
3. Unstuff R378 for double pull-down
4. Unstuff R596 for leakage issue
5. Unstuff R567 for level issue
6. Change DPWROK from DPWROK to RSMRST#
7. Unstuff DSW power ok circuit
8. Add C657 for EMI request
9. Add R294 for Intel suggest
10. Unstuff JTAG debug circuit
11. Unstuff U10 & R303, R308, R307, R315, R321.
12. Add R631 for Intel suggest
13. Change C648 & C649 for vendor suggest
14. Remove 27MHz for GPU clock
15. Change board ID 1 to INT_BT_COMBO_EN#
16. Add GPIO68 for RF_POWER OFF control
17. Change BOARD ID 2 to pull high
18. Unstuff R158
19. Unstuff R269 because double pull high
20. Unstuff C329 for leakage issue
21. Unstuff C419 & C418 for cost down
22. Unstuff R431 because double pull-high
23. Change C132 & C141 for vendor suggest
24. Unstuff R37 for double pull-high
25. Change R444 for N12P-GV setting
26. Change R456 for N12P-GV setting
27. Add R402 for strap4 setting
28. Add R464 for strap3 setting
29. Add C656 for EMI
30. Add R287 to share CRT power to HDMI
31. Add C658 for EMI
32. cHANGE CN4 PN
33. Change R6 pull high voltage to +5VS5
34. Add LVDS1 GND
35. Add R637 for cost down
36. Change R335 pull high voltage to +5V
37. Unstuff U11 for cost down
38. Change R344 & R322 to +5VAVDD
39. Add C655 for EMI
40. Add R638 to connect +5VAVDD to +5V_AVDD
41. Add R636 to connect +3V_AUDIO to +3V
42. Unstuff R234 for leakage issue
43. Add R639 as vendor suggest
44. Add PQ54 for leakage issue
45. Add C654 & C653 for EMI
46. Change R191, R192, R557, R556, R193, R194, R196, R197 to 0402 size
47. Unstuff R268 for power consumption issue
48. Add R459 for Intel combo card contorl switchable
49. Change combo card power control source to PCH (stuff R359)
50. Add Q56 for combo card BT control logic
51. Change R355, R354 & C478 to +3VPCU
52. Add C385 for EMI
53. Stuff L6 & L5 for USB
54. Change C644 PN
55. Unstuff LAN_S5_WAKE# for control host change
56. Unstuff R80 & R81 for pull-high voltage issue
57. Unstuff thermal shutdown circuit
58. Add D30 for ME lock issue
59. Change CN2 PN & footprint
60. Add PD18 & PR233 for GPU power on/off sequence control
61. Unstuff PD10 for cost down
62. Change PQ12 control signal to DGPU_PWR_EN
63. Add PC543 for Intel suggest
64. Unstuff U5
65. Unstuff R242 & stuff R246 and D11 for contorl host change
66. Change D3 PN for leakge issue

